Design Guide

Version 1.1 November, 2016

REVISION HISTORY

Rev	Date	Notes
0.1	Jan 29, 2016	Initial release
1.0	March 2nd, 2016	First Release
1.1	Sep 9, 2016	Change UART, I²S and SDIO to 3.3V

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1. Introduction

1.1 General Introduction

M2.COM is a sensor module platform with a simple design that provides a solid, standard platform for IoT nodes and sensors. The basic M2.COM concept is for a standard form factor that combines sensor, embedded system, and networking all in one device. With the utilization of M2.COM, development times and resources are reduced. The modular design makes it flexible enough to support different applications through an I/O switching sensor or the M2.COM module itself and this opens up possibilities for deploying more sensors and fulfilling more demands in the IoT world.

M2.COM adopts the M.2 form factor with a 75-position host interface connector, sufficient to support all the I/O features inside the M2.COM multi-function module. The compact size of only 30 mm in length and 22 mm in width is very convenient for micro sensor implementation and system integration. For demanding projects that will not fit into the standard 30 x 22 mm, we also offer an extended M2.COM module at 42 mm in length and 30 mm in width.
M2.COM supports multiple I/O features for data collection and device control, including: USB, PWM, SDIO, I²C, I²S, UART, GPIO, SPI and ADC. Providing maximum pin-out flexibility, customers can easily connect various sensors and control end devices with the M2.COM sensor module platform.

1.2 Purpose of This Document

This document provides design recommendations for an M2.COM Carrier Board, which is based on an M2.COM Module. It identifies the hardware and RF integration aspects that must be considered when designing a platform or application.

The document is written for system hardware engineers. It also addresses SDK and OS/Software issues wherever applicable. This guide is intended to aid hardware and RF designers, to help them understand the applications of the modules they are developing and the M2.COM infrastructure.

***Note**: This document is based on the existing industry specifications, which may be revised and upgraded. All information specified is preliminary, based on current expectations, and is subject to change without notice.*

1.3 Design Support

There are a number of ways to develop a M2.COM Carrier board:

- Consult with your M2.COM module vendor to review your design; they may have

their own design checklist. Make sure also to have the appropriate semiconductor companies review the portions of the design that utilize their components, or follow their application and design guidelines.

- Use a 3rd party firm that specializes in M2.COM Carrier Board development.
- Contact your M2.COM module vendor. The module vendor may have an FAE available for advice. Many vendors undertake custom carrier board design projects for significant opportunities.

1.4 Abbreviations and Acronyms Used

- **ADC** Analog to Digital Converter
- **ARM** Advanced RISC Machines **www.arm.com**
- **BSP** (Software) Board Support Package
- **CAD** Computer Aided Design
- **CAN** Controller Area Network
- **CODEC** Coder – Decoder
- **DAC** Digital to Analog Converter
- **DB-9** Connector, D shaped, B shell size, 9 pins
- **DE** Differential Ended (signal pair)
- **DNI** Do Not Install (component is not loaded)
- **EEPROM** Electrically Erasable Programmable Read Only Memory
- **eMMC** Embedded Multi Media Card **www.jedec.org**
- **ESD** Electro Static Discharge
- **FET** Field Effect Transistor
- **FIFO** First In First Out (buffer memory)
- **FS** Full Speed (USB 2.0 12 Mbps)
- **GPIO** General Purpose Input / Output
- **HDA** High Definition Audio – Intel defined format **www.intel.com**
- **HS** High Speed (USB 2.0 480 Mbps)
- **IC** Integrated Circuit
- **I^2C** Inter-Integrated Circuit **www.nxp.com**
- **I^2S** Inter-Integrated Circuit – Sound **www.nxp.com**
- **IO** Input Output
- **ISO** International Organization for Standardization (French) **www.iso.org**
- **JEDEC** Joint Electron Device Engineering Council **www.jedec.org**
- **JPEG** Joint Photographic Experts Group **www.jpeg.org**
- **LED** Light Emitting Diode

- **M2.5** Metric 2.5mm
- **M3** Metric 3.0mm
- **Mbps** Megabits per second
- **MLC** Multi Level Cell (Flash Memory Reference)
- **MPEG** Motion Picture Experts Group **www.mpeg.org**
- **NAND** A high density flash memory technology
- **nS** Nano second (10 E -9)
- **NC** Not Connected
- **NXP** A semiconductor company **www.nxp.com**
- **OS** Operating System
- **OTG** On the Go (USB term – device can be host or client)
- **PCB** Printed Circuit Board
- **PCM** Pulse-Code Modulation
- **PLL** Phase Locked Loop
- **pS** Pico second (10 E -12)
- **PWM** Pulse Width Modulation
- **RISC** Reduced Instruction Set Computing
- **ROM** Read Only Memory
- **RS232** Recommend Standard 232 (asynch serial ports)
- **RS485** Asynchronous serial data, differential, multi drop
- **RTC** Real Time Clock (battery backed clock and memory)
- **SAR** Successive Approximation Register
- **SD** Secure Digital (memory card)
- **SDK** Software Development Kit
- **SE** Single Ended (signal, as opposed to differential)
- **SLC** Single Level Cell (flash memory reference)
- **SOC** System On Chip
- **SPI** Serial Peripheral Interface
- **TI** Texas Instruments – semiconductor company **www.ti.com**
- **UART** Universal Asynchronous Receiver Transmitter
- **UL** Underwriters Laboratories **www.ul.com**
- **USB** Universal Serial Bus **www.usb.org**
- **X5R** Ceramic capacitor dielectric – Capacitance tolerance +-10% and Operation temperature -55C~85C
- **X7R** Ceramic capacitor dielectric – Capacitance tolerance +-10% and Operation temperature -55 °C~125 °C

1.5 Reference Document

1.5.1 M2.COM Specification V1.1, Nov, 2016.

1.5.2 Industry Standards Documents

- **eMMC ("Embedded Multi-Media Card")** the eMMC electrical standard is defined by JEDEC JESD84-B51 and the mechanical standard by JESD84-C44 (**www.jedec.org**).
- **SD Specifications Part 1 Physical Layer Simplified Specification,** Version 4.01, Jan 22, 2013, © 2010 SD Group and SD Card Association ("Secure Digital") (**www.sdcard.org**).
- **CAN ("Controller Area Network")** Bus Standards – ISO 11898, ISO 11992, SAE J2411.
- **The I^2C Specification,** Version V6, April 04 2014, Philips Semiconductor (now NXP) (**www.nxp.com**).
- I^2S **Bus Specification,** Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (**www.nxp.com**).
- **RS-232** (EIA "Recommended Standard 232") this standard for asynchronous serial port data exchange dates from 1962. The original standard is hard to find. Many good descriptions of the standard can be found on-line, e.g. at Wikipedia, and in text books.
- **SPI Bus –** "Serial Peripheral Interface" – de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (**http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus**).
- **USB Specifications** (**www.usb.org**).

1.6 Schematic Example Correctness

The schematic examples shown in this Design Guide are implemented to be working correctly-although correctness can't be guaranteed for all applications. Most of the examples have been applied to the Demo Carrier Board and have been built, tested, and are verified to work.

1.7 OS and Software SDK Support

M2.COM supports all the necessary software stacks to build up IoT sensor devices. The ARM mbed or RTOS is the foundation of the embedded micro sensor operating system, with supporting multiple IoT communication protocols including LWM2M, OSGI, AllJoyn and MQTT. Data can be quickly and easily acquired and transformed into a different formats defined by cloud service providers. Module makers may provide a web configuration service, SDK and User Manual to help set up the environment and speed up development IoT sensor devices.

1.8 Schematic Example Conventions

Some of the conventions used in the examples are described below. The symbol of Off-page has a number index to connect to the schematic page.

Figure 1 Schematic Symbol Conventions

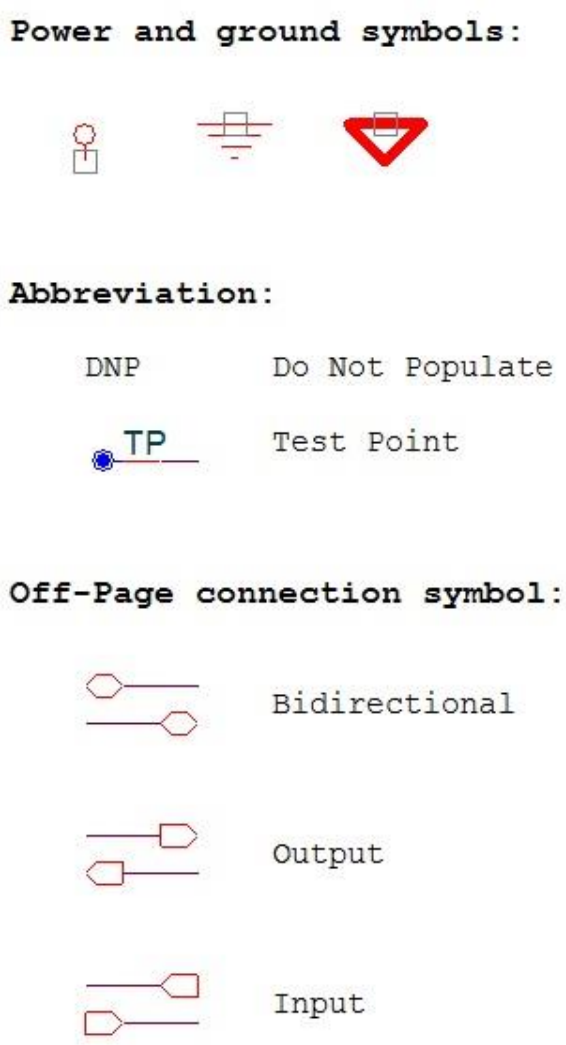


Table 1 Schematic Power Naming

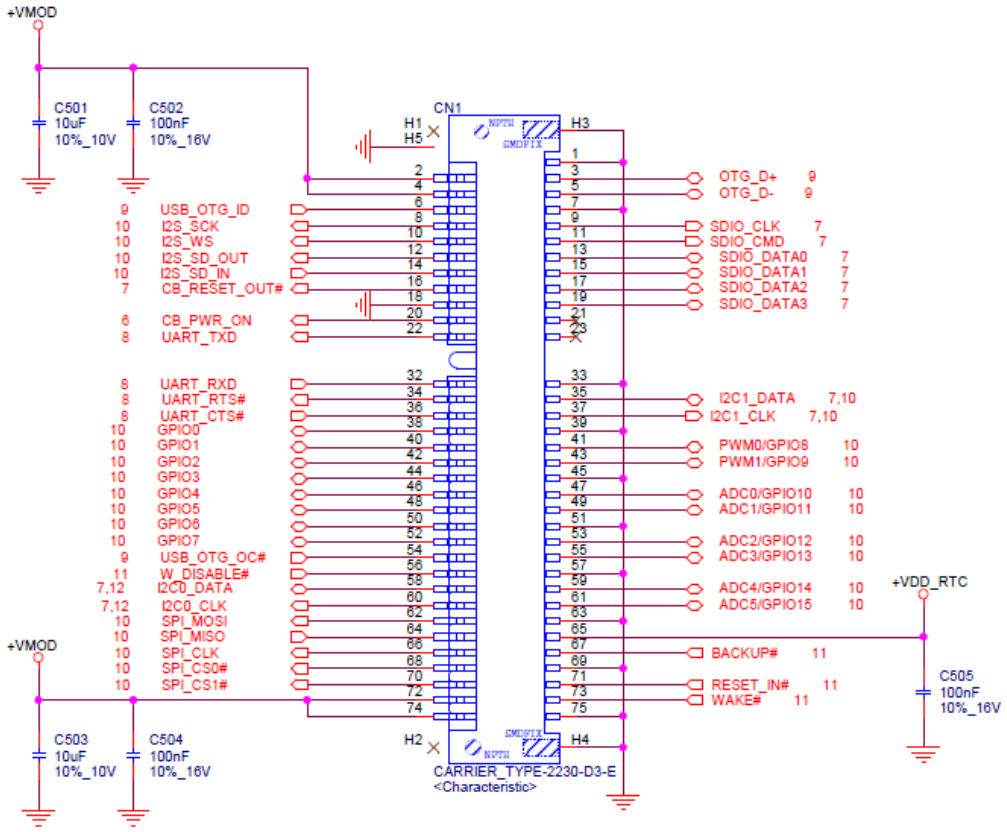
+ADP_IN	Power source for the overall system. Before DCDC converter without UVP and OVP protection circuit.
+VMOD	Main power to M2.COM module. Voltage is 3.3V.
+VDD_RTC	RTC backup power to M2.COM module.
+V3.3	3.3V IO power supply.
+V5	5V USB power supply.

2. Infrastructure: Connector, Power Delivery, System Management

2.1 Module Connector

M2.COM Module Connector adopts the type 2230 or 3042 M.2 form factor with a 75-position host interface connector, and supports H3.2-D3 or H4.2-D5 connectors. Pin definitions are shown below.

Figure 2: Connector Pins 1 to 75 and H1 to H5



2.2 Module Power

2.2.1 Input Voltage Range

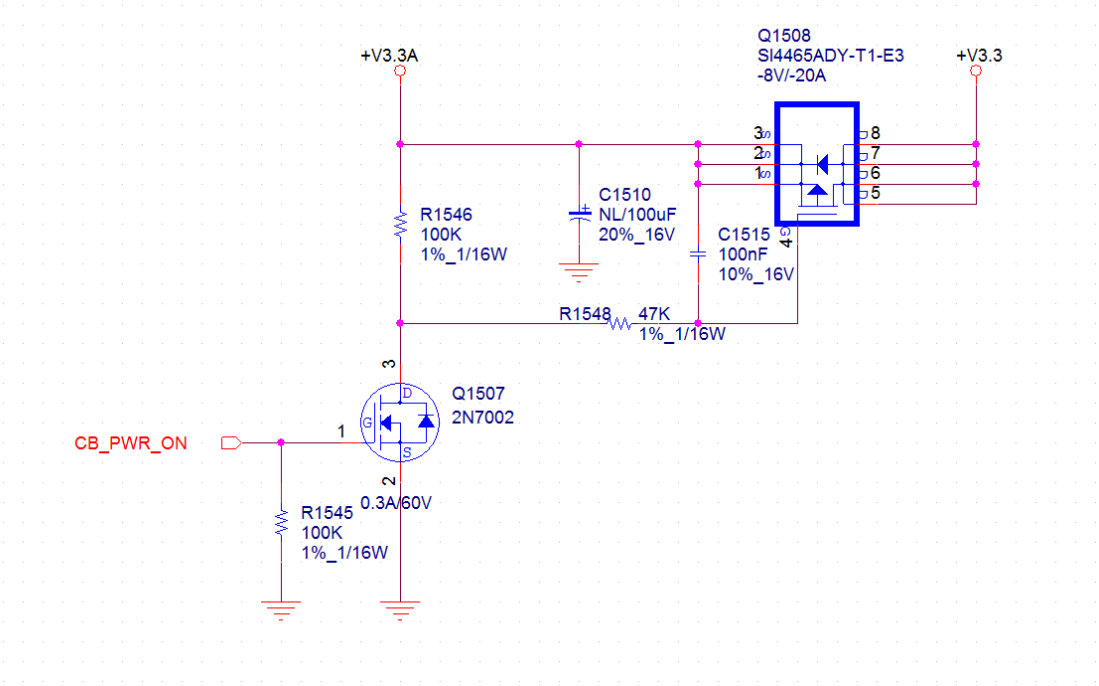
M2.COM modules accept input power voltages from 3.15V to 5.25V. Power Input can use fixed 3.3V to the module power pins. The carrier board can use a DC converter to provide 3.3V for M2.COM module.

2.2.2 Input Voltage Rise Time

There is no set value in the module HW specification on the power supply Rise Time. Some power rails may add big input capacitors for the transient response to reduce rippling on the

power rails. When the system powers on at the initial T0 state, input capacitors create a surge current in the power supply, and this may overpower some of the components (MOSFET Pd) or the DC converter over-current protection function. So we recommend adding a soft-start circuit to reduce surge currents at the initial state as below. You can adjust the RC circuit to fine tune the Rise Time and surge current if there is a specific requirement on the Rise Time value.

Figure 3 Soft-Start Circuit on the Power rail



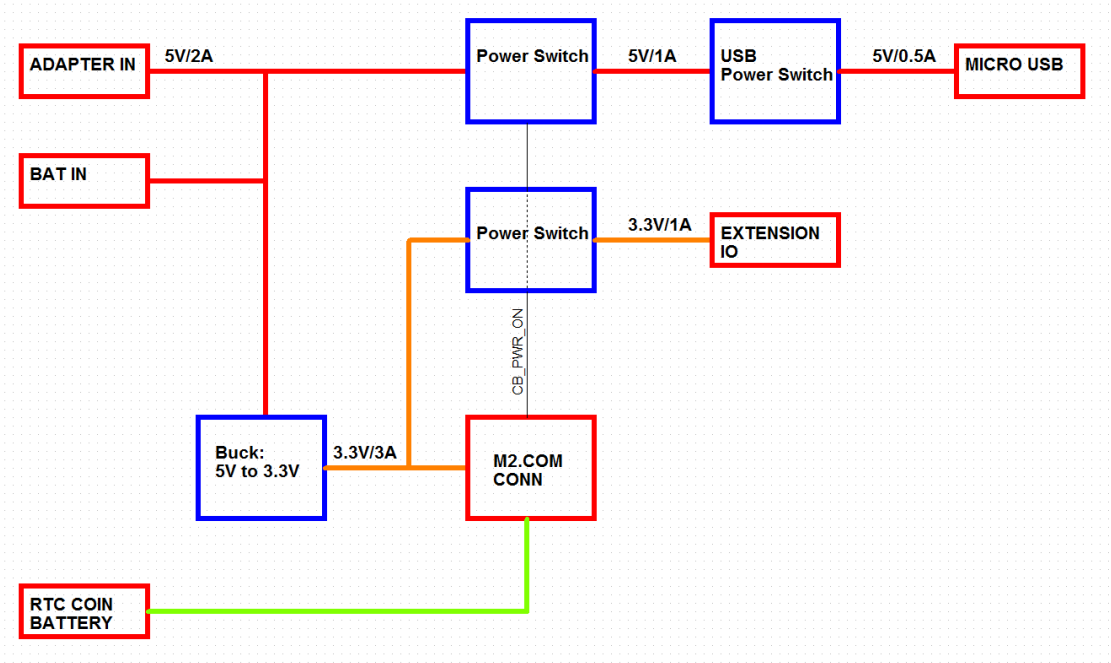
2.2.3 Module Maximum Input Power

The M2.COM specification document states that the input voltage range is 3.15V to 5.25V. Each M2.COM connector pin is able to carry 0.5A maximum current. The M2.COM module allocates 4 pins for input power and 11 pins for ground. Allow 2A max at +3.15V with 6.3W. You may consider derating the wattage to 80% and the maximum input power to 5 watt. Most IoT nodes and sensors applications may be under 0.5 watts. Power saving is a key success factor for IoT nodes and sensors.

2.2.4 Power Path

The power path for a basic input voltage and DC converter arrangement for the M2.COM carrier board is shown in Figure 4 below. The figure also shows carrier board power supply sections assuming a typical system powered by power source fixed at 5V. However, you may design the variable 3.3V to 5V range. This power path is an example; you can customize your power path design to be optimized for specific applications.

Figure 4 Basic Module and Carrier Power Path



2.3 Module I/O Power

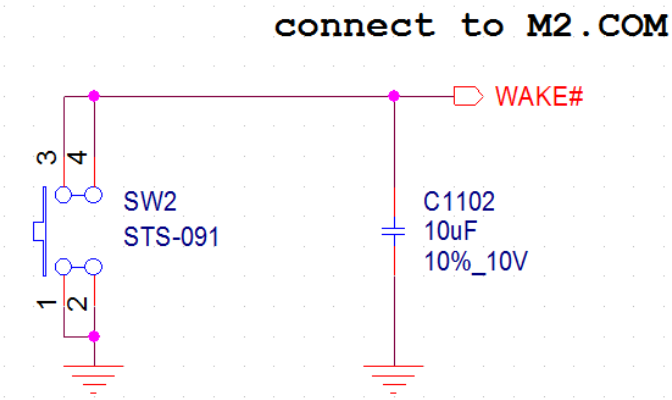
M2.COM supports 3.3V I/O buffer. SDIO, I^2S, SPI, **I^2C**, GPIO and Management pins are 3.3V I/O on module.

***Note**: M.2 I/O (NGFF) is not fully pin-to-pin compatible with the M2.COM module I/O power. M.2 I/O interfaces with X86 platforms that use .14u and 1.8V I/O CPU or PCH. Installing a M2.COM module to a M.2 (NGFF) may damage your platform.*

2.4 WAKE#

IoT nodes and sensors usually have sleep or shutdown modes to save power. WAKE# is an external event to wake up the MCU or sensors when data uploads are needed. We recommend adding a debouncer circuit on the module.

Figure 5 Wake# Button



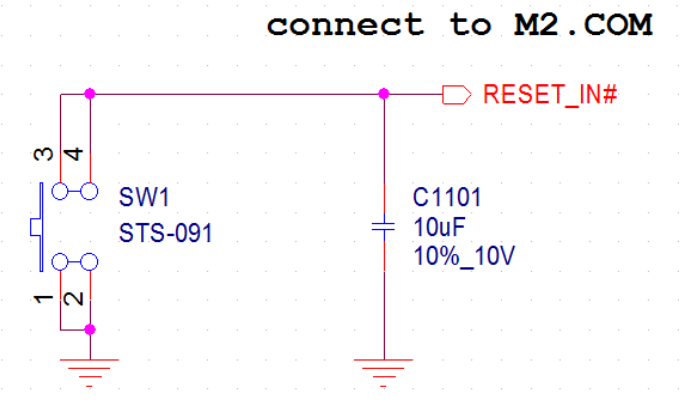
2.5 CB_PWR_ON

In order to make sure all power rails on the M2.COM module are ready for all devices, and the module power rails and the SOC are ready, the MCU on the module will release CB_PWR_ON to power on the carrier board power rails.

2.6 RESET_IN# and CB_RESET_OUT#

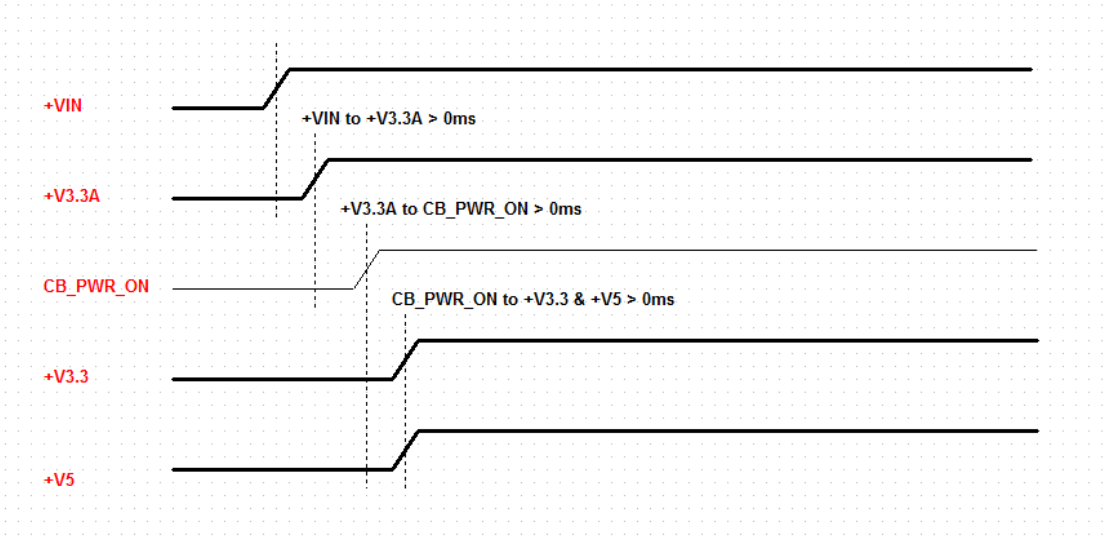
The RESET_IN# signal may be used to force a M2.COM system reset. It is an input to the module that pulls up resistance on the module with a debounce circuit. If implemented by the carrier board, request an open drain circuit or a switch to GND should be used. An example is show below.

Figure 6 Reset Button



2.7 Power-up Sequence

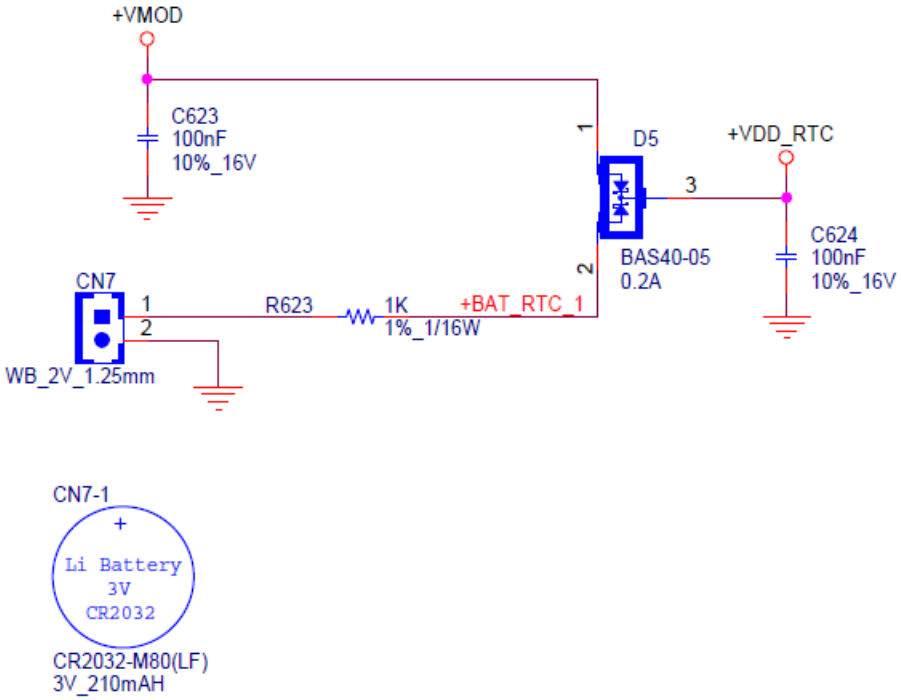
Figure 7 Power-up Sequence



2.8 RTC Backup Power

+VDD_RTC is a backup power plane for a system power shutdown in order to back up data to a Cloud.

Figure 8 RTC and CMOS circuit



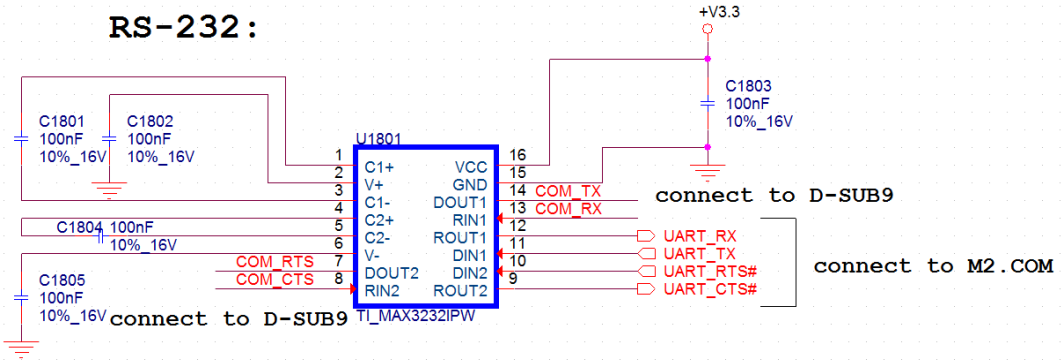
3. Low/Medium Speed Serial I/O Power Interfaces

3.1 Asynchronous Serial Ports

3.1.1 RS232 Ports

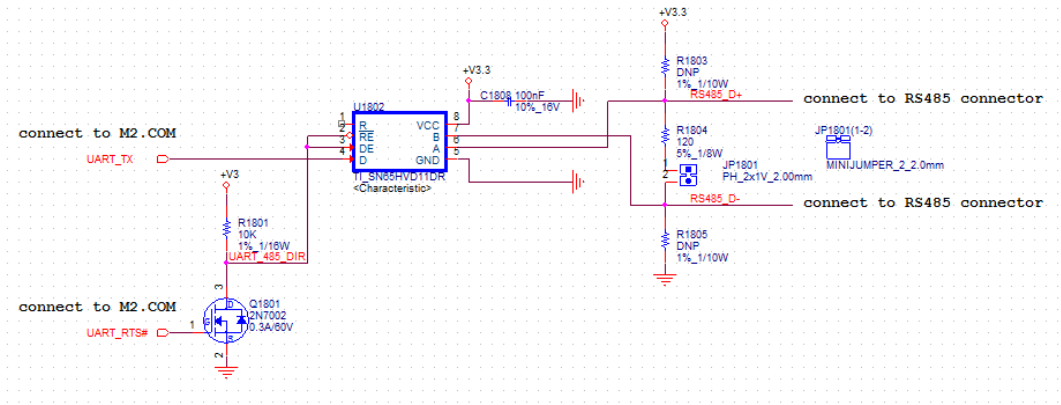
The M2.COM module asynchronous serial ports run at a default of 3.3V I/O logic levels. The transmit and receive data lines to and from the module are active high, and the handshake lines are active low. If the asynchronous ports are to interface with RS232 level devices, then a carrier RS-232 transceiver is required. The logic side of the transceiver must be able to run at 3.3 I/O levels. The selection of 3.3v I/O compatible transceivers is a requirement. The Maxim MAX3232 device is illustrated in the figure below. The MAX3232 can operate at a maximum speed of 1 Mbps. The transceivers invert the polarity of the incoming and outgoing data and handshake lines.

Figure 9 RS232



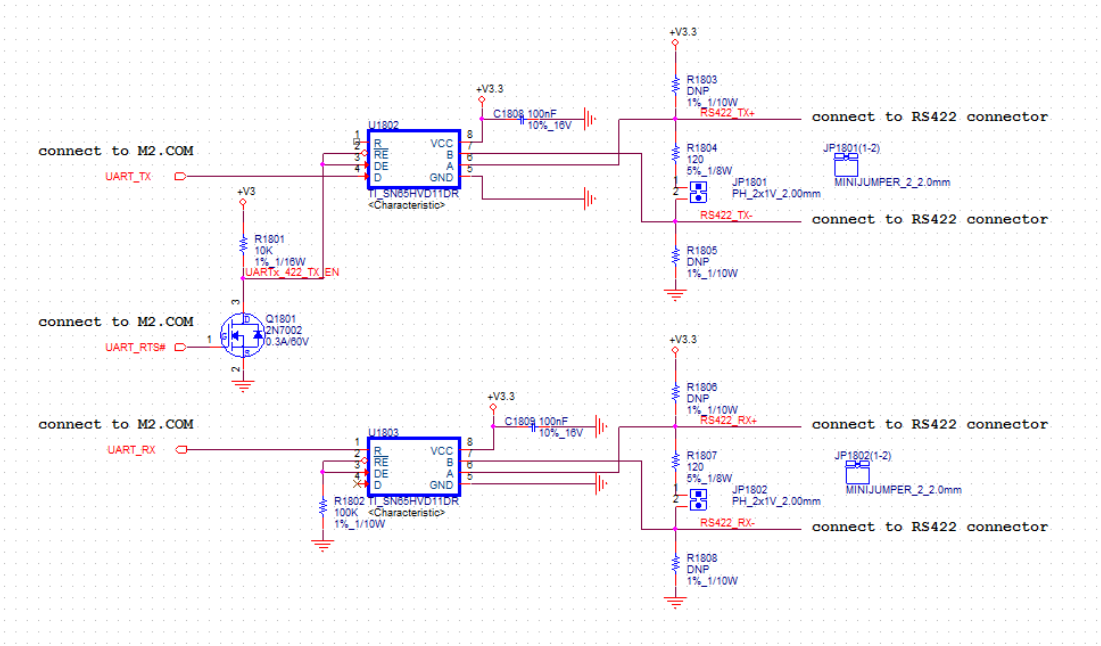
3.1.2 RS485 Half-Duplex

Figure 10 RS485



3.1.3 RS422 Half-Duplex

Figure 11 RS422



3.2 I²C Interfaces

3.2.1 General

The I²C-bus is a de facto world standard that is now implemented in over 1000 different ICs manufactured by more than 50 companies. Additionally, the versatile I²C-bus is used in various control architectures such as System Management Bus (SMBus), Power Management Bus (PMBus), Intelligent Platform Management Interface (IPMI), Display Data Channel (DDC) and Advanced Telecom Computing Architecture (ATCA).

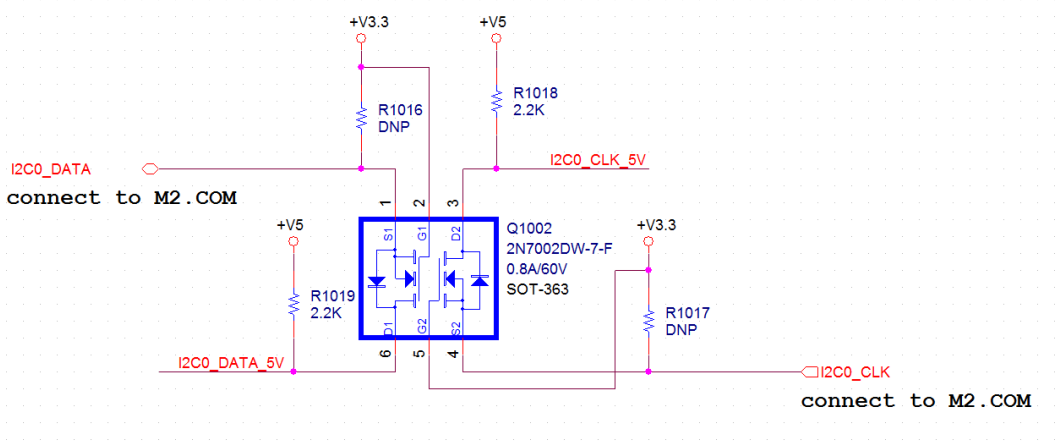
Here are some features of the I²C-bus:

- Only two bus lines are required; a serial data line (SDA) and a serial clock line (SCL).
- Each device connected to the bus is software addressable by a unique address and a simple master/slave relationship exists at all times; masters can operate as master-transmitters or as master-receivers.
- It operates as a true multi-master bus, including collision detection and arbitration to prevent data corruption if two or more masters simultaneously initiate data transfer.
- Serial, 8-bit, bi-directional data transfers can be made at up to 100 Kbit/s in Standard-mode, up to 400 Kbit/s in Fast-mode, or up to 1 Mbit/s in Fast-mode Plus. Also, up to 3.4 Mbit/s in High-speed mode and serial, 8-bit oriented, unidirectional data transfers up to 5 Mbit/s in Ultra-Fast-mode. On-chip filtering rejects spikes on the bus data line to preserve data integrity. The number of ICs that can be connected to the same bus is limited only by the maximum bus capacitance. More capacitance may be allowed under some conditions.

3.2.2 I²C Level Transition, Isolation and Buffering

MOSFET is one of methods to level shift from 5v to 3.3v as shown in the figure below. Review MOSFET Vgs on voltage to meet your level shift requirement and body diode direction to avoid voltage leakage when the system suspends different power rails.

Figure 12 I²C Level Shift



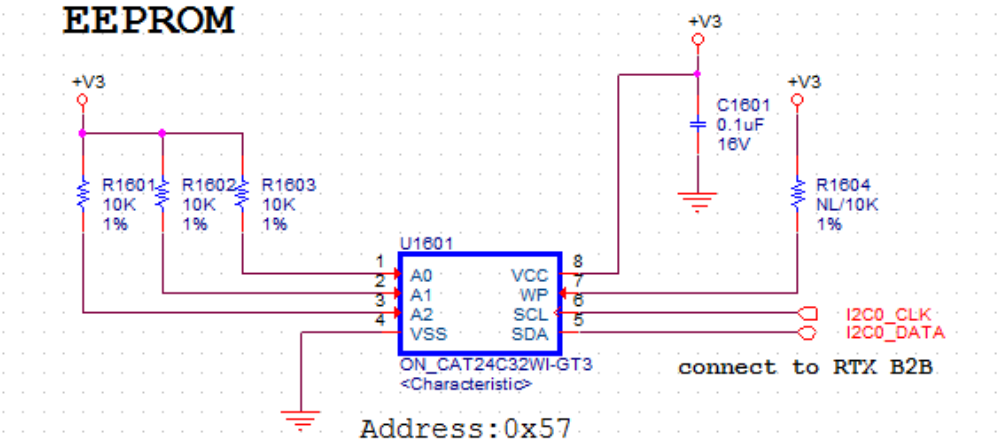
3.2.3 I2C_PM Bus EEPROMs

The module I²C is rated at 3.3v and draws 3.3v inside, with each power rail at 3.3v. The layout topology of the I²C bus is daisy chain. I²C operates Standard-mode (100 Kbit/s), Fast-Mode (400 Kbit/s), Fast-mode Plus (1 Mbit/s) and High-speed mode (3.4 Mbit/s) for Bi-direction bus. For instance, Fast-mode Plus (FM+) devices offer an increase in I²C-bus transfer speeds and total bus capacitance. Fm+ devices can transfer information at bit rates of up to 1 Mbit/s, yet they remain fully downward compatible with Fast- or Standard-mode devices for bidirectional communication in a mixed-speed bus system. The same serial bus protocol and data format is maintained as with the Fast- or Standard-mode system. Fm+ devices also offer increased drive current over Fast- or Standard-mode devices allowing them to drive longer and/or for more heavily loaded buses so that bus buffers do not need to be used. The drivers in Fast-mode Plus parts are strong enough to satisfy the Fast-mode Plus timing specification with the same 400 pF load as Standard-mode parts. To be backward compatible with Standard-mode, they are also tolerant of the 1 µs rise time of Standard-mode parts. In applications where only Fast-mode Plus parts are present, the high drive strength and tolerance for slow rise and fall times allow the use of larger bus capacitance as long as they are set-up with minimum LOW time and minimum HIGH time for Fast-mode Plus, and the fall time and rise time do not exceed the 300 ns tf and 1 µs tr specifications of Standard-mode. Bus speeds can be traded against load capacitance to increase the maximum capacitance by about a factor of ten.

3.2.4 General I²C Bus EEPROMs

Other I²C buses (I2C0_CLK, I2C0_DATA) operate at 3.3v I/O. The Power rail is 3.3v so no need to add level shift.

Figure 13 EEPROM I²C

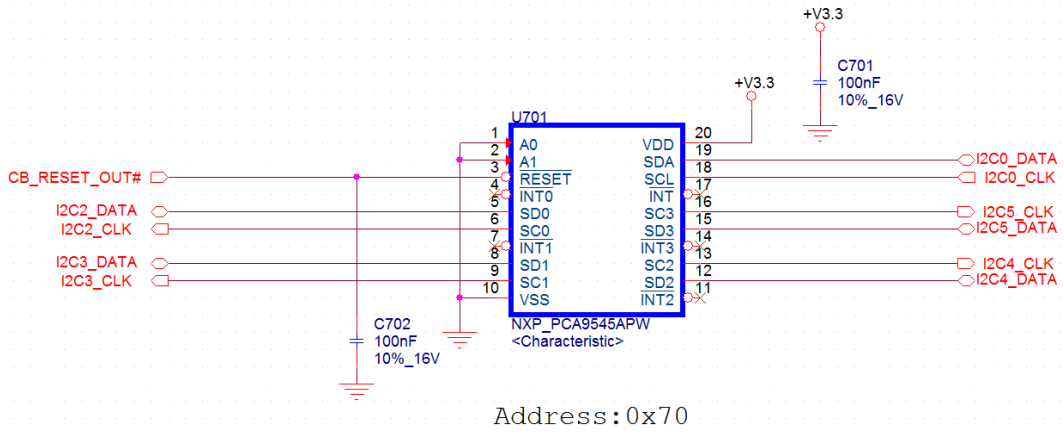


3.2.5 I²C Based IO Expanders

I²C has 4-channel I²C bus switch device to expand I²C bus and I/O devices. NXP/TI PCA9545A/45B/45C is a quad bidirectional translating switch controlled via the I²C -bus. The SCL/SDA upstream pair fans out to four downstream pairs, or channels. Any individual SCx/SDx channel or combination of channels can be selected, determined by the contents of the programmable control register. Four interrupt inputs, INT0 to INT3, one for each of the downstream pairs, are provided.

An active LOW reset input allows the PCA9545A/45B/45C to recover from a situation where one of the downstream I²C -buses is stuck in a LOW state. Pulling the RESET pin LOW resets the I²C -bus state machine and causes all the channels to be deselected as does the internal power-on reset function. The pass gates of the switches are constructed such that the VDD pin can be used to limit the maximum high voltage which is passed by the PCA9545A/45B/45C.

Figure 14 I²C IO Expanders



3.3 I²S Interfaces

3.3.1 General

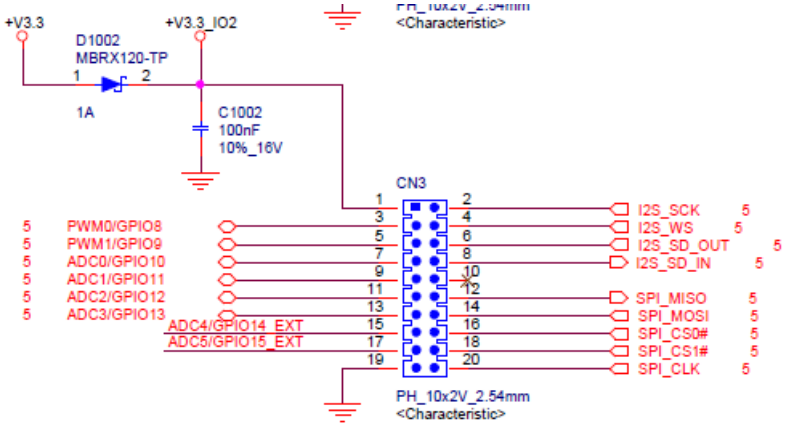
This standard was introduced in 1986 by Philips (now NXP) and was last revised in 1996. The I²S protocol outlines one specific type of PCM digital audio communication with defined parameters outlined in the Philips specification. The bit clock pulses once for each discrete bit of data on the data lines. The bit clock frequency is the product of the sample rate, the number of bits per channel and the number of channels.

3.3.2 M2.COM Carrier board reference design

M2.COM carrier board reserves Pin header CN3 for the I²S interface. The driver of the I²S device is not available for now. This Extended IO interface (Pin header) has space reserved for future design and extension.

***Note**: Many I²S devices might not support driver for ARM mbed or RTOS. Consider your own driver support for I²S solutions.*

Figure 15 Pin Header for I²S, SPI, PWM and ADC interface



3.4 SPI Interface

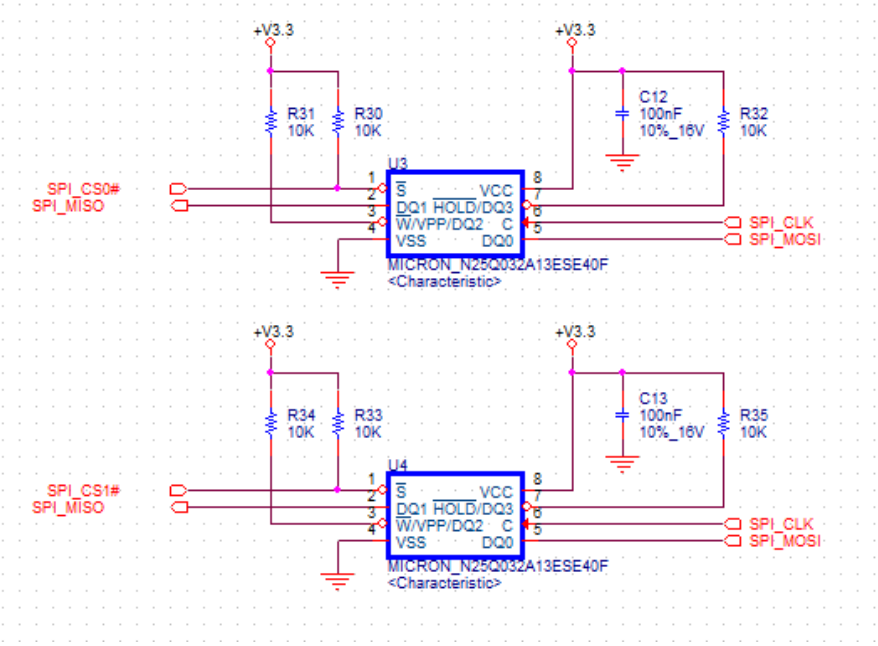
3.4.1 General

The Serial Peripheral Interface (SPI) bus is a full duplex synchronous serial communication interface specification used for short distance communication. The interface was developed by Motorola and has become a de facto standard. SPI devices communicate in full duplex mode using a Master-Slave architecture with a single master. The master device originates the frame for reading and writing. Multiple slave devices are supported through selection, with individual slaves selected by CS lines.

3.4.2 M2.COM Implementation

The M2.COM Module may be configurable as a SPI master or slave depending on the application, with two SPI devices on M2.COM Modules that can be used. The SPI interface could be an external serial flash or application processor that needs to be configurable to different memory maps for the MCU. Please refer to the M2.COM module vendor solution and spec to setup an API document.

Figure 16 SPI Interface on Pin Header



3.5 CAN Bus

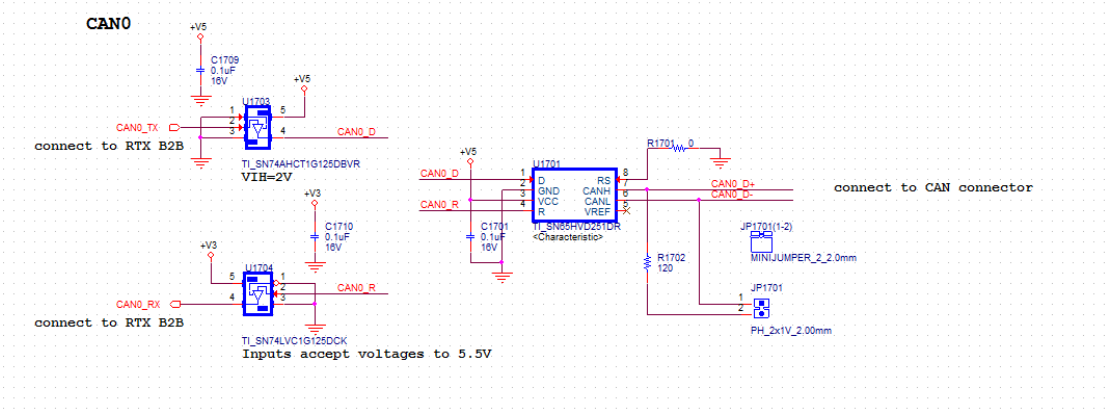
3.5.1 General

The Controller Area Network (CAN) is a serial communications protocol that efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high speed networks to low cost multiple wiring. The maximum signaling rate is 1 Mbps.

3.5.2 M2.COM Implementation

CAN Bus is multi-functional on the M2.COM spec with UART TXD and RXD. It can support 2 logic level CAN ports. A carrier board is required to implement CAN PHY as below. This demo circuit shows 120-ohm terminations across the CAN pair.

Figure 17 CAN Bus transceiver



3.5.3 Isolation

The ISO 1050 is a galvanically isolated CAN transceiver that meets the specification ISO11898-2 standard. The device has logic input and output buffers separated by a silicon oxide (SiO2) insulation barrier that provides galvanic isolation of up 5000 Vrms for 1050DW and 2500 Vrms 1050DUP.

3.6 JTAG

The M2.COM spec does not define the JTAG function on the M2.COM connector interface. The M2.COM module vendor may implement JTAG on their module for development. Please consult with the M2.COM module vendor for information about this feature.

4. High Speed Serial I/O Interfaces

4.1 USB Bus

4.1.1 General

The USB (Universal Serial Bus) is a hot-pluggable general purpose high speed I/O standard for computer peripherals. The standard defines connector types (Type A, Type B, Mini-A, Mini-B, Micro-A and Micro-B), cabling, and communication protocols for interconnecting a wide variety of electronic devices.

The USB 2.0 Specification defines data transfer rates of 480 Mbps (High Speed USB). A USB host bus connector uses 4 pins: a power supply pin (5V) with 500mA, a differential pair (D+ and D- pins) and a ground pin. Additionally a fifth pin, USB ID for USB-OTG that may be used which indicates whether the device operates in Host mode or Client/Device mode.

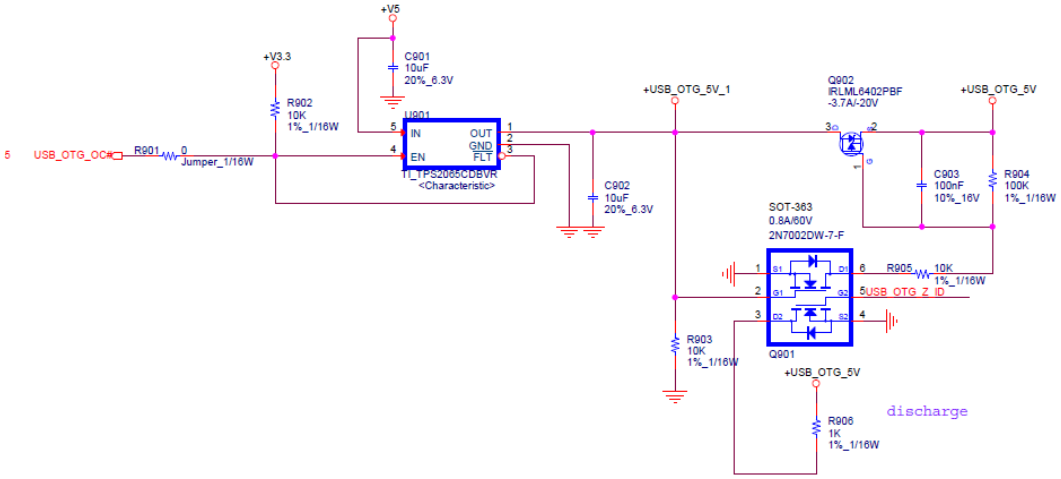
M2.COM modules support USB 2.0 and USB OTG functions. The USB 2.0 port can be configured as a host, client or OTG port. OTG operation is optional.

4.1.2 USB OTG

Figure 18 shows a USB-OTG implementation on the USB 2.0 port on a Mini USB Type B connector. The ESD diodes should be placed close to the connector, and the USB differential traces routed as differential pairs in “no stub” topology. The common choke on differential pairs can reduce common mode emissions for EMC radiation.

The module USB_OTG_PWR_EN# signal controls the power switch with short circuit protection. The Texas Instruments TPS2065 module’s current limit is between 1A and 1.9A. 70m ohms Rds on resistance can help the voltage drop.

Figure 18 USB -OTG

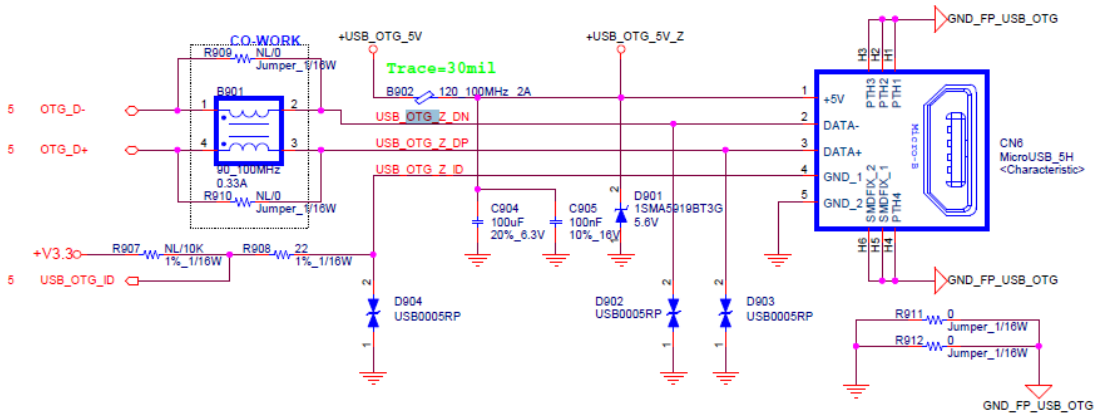


4.1.3 USB 2.0 Host Ports

Figure 19 shows the carrier board implementation of USB 2.0. The ESD diodes should be placed close to the connector and low capacitance to reduce the signal integrity of USB 2.0. The USB differential traces are routed as differential pairs in a “no stub” topology. The common choke on a differential pair can reduce common mode emissions for EMC radiation.

The module USB_OTG_ID signal controls the power switch with short circuit protection, the Texas Instruments TPS2065 module’s current limit is between 1A and 1.9A. 70m ohms Rds on resistance can help voltage drop.

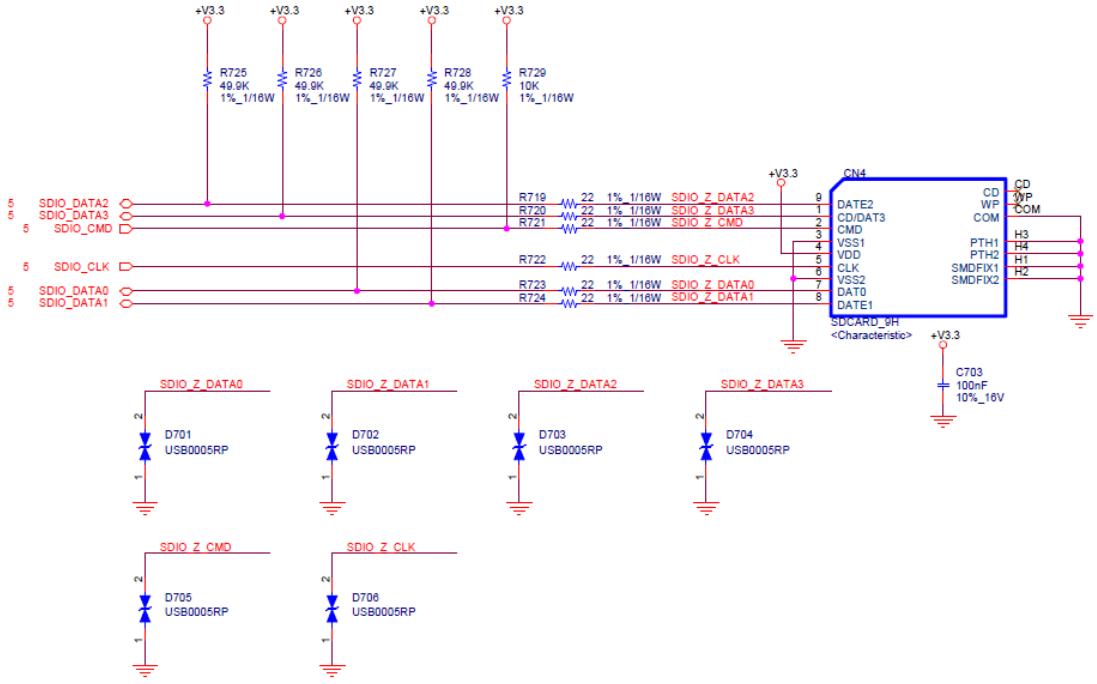
Figure 19 USB 2.0 Implementation



4.2 SD Card

The SD card is a memory card that is specifically designed to meet security, capacity, performance, and environment requirements inherent in newly emerging audio and video applications. The SD standard is maintained by the SD Card Association. In addition to the SD Memory Card, there is the SD I/O (SDIO) Card. The SDIO Card specification is defined in a separate specification named: "SDIO Card Specification" that can be obtained from the SD Association. The SD Memory Card communication is based on an advanced 9-pin interface (Clock, Command, 4 x Data and 3 x Power lines) designed to operate at a maximum operating frequency of 50 MHz and low voltage ranges. The M2.COM module supports SDIO 3.3V I/O.

Figure 20 SD Card



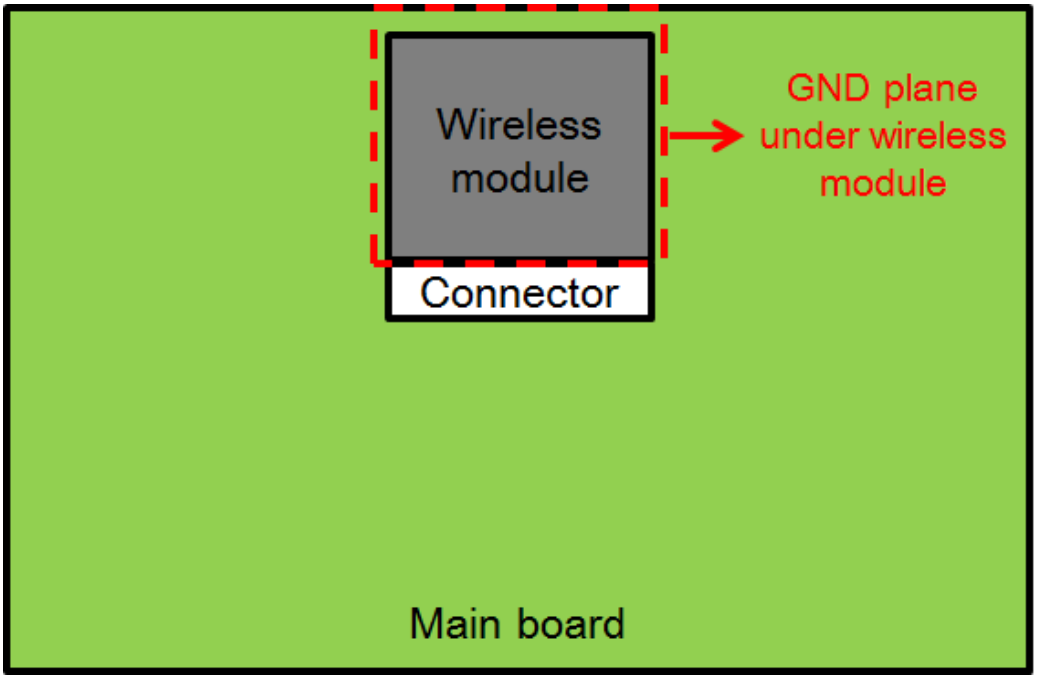
5. RF Integration Recommendations

5.1 M2.COM Module Placement

RF module placement is very important for the wireless transmission and received performance. The following suggestion lists the considerations for the RF module placement.

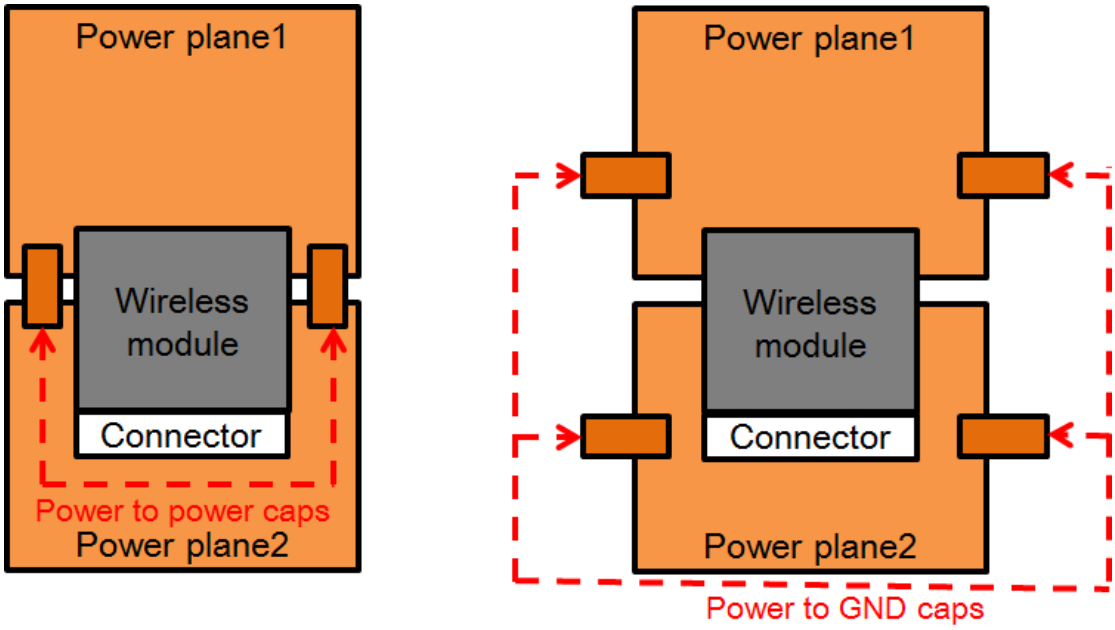
1. The RF module should be placed near the edge of the carrier board to reduce antenna cable length and avoid noise interference issues.
2. The RF module should be far from the high speed digital IC, Switching Power Supply (Power IC) and power chokes that are noisy and their harmonic frequency interferences with the RF performance and sensitivity.
3. Adding a continuous GND plane under the RF module helps to avoid noise interference in the radio band.

Figure 21 GND plane under RF module



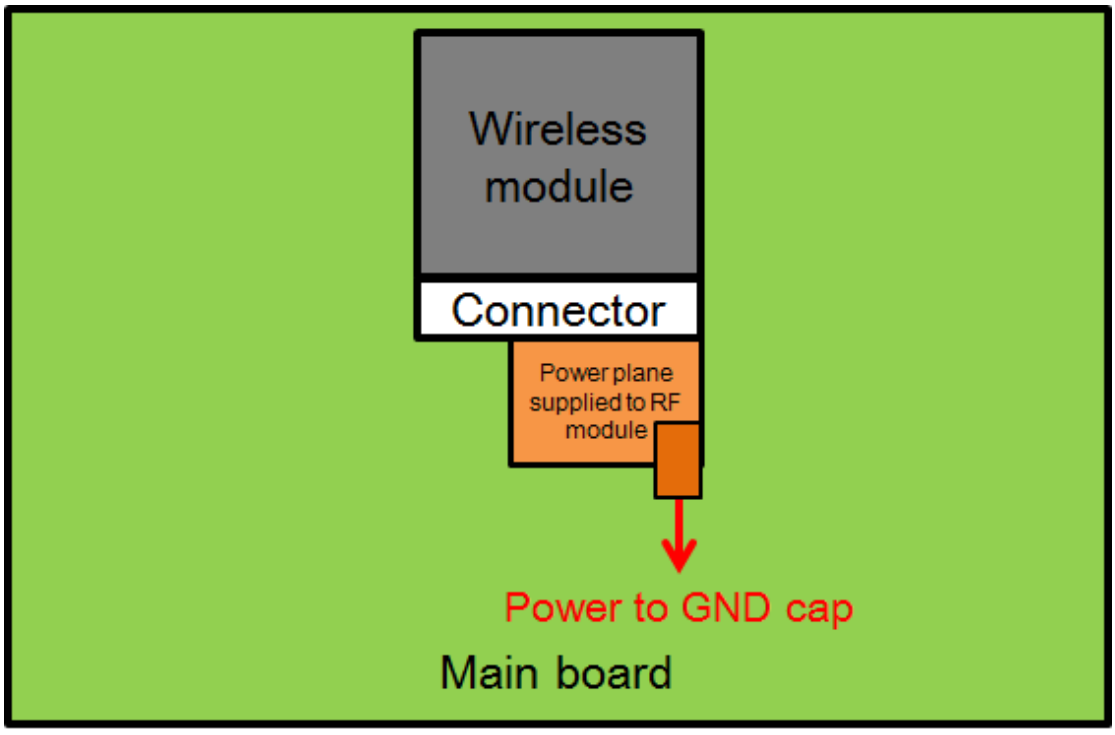
4. If power plane is plated under the RF module, please reserve “power to power” and “power to GND” stitching caps around the power plane to filter band noise.

Figure 22 Stitching caps on the power plane



5. Please reserve a stitching cap on the power plane supplied to the RF module for noise reduction.

Figure 23 Reserve cap on the power plane supplied to the RF module



6. All high speed connectors that are USB 2.0, CAN Bus, and SD card should be far from RF circuits and antenna.
7. High speed traces that are USB 2.0, CAN Bus, SDIO and SPI should be far from RF circuits, and should not run these traces underneath the RF module.

5.2 Layout Guidelines

A bad PCB layout may produce unwanted noise that reduces received wireless sensitivity. The noise may interfere with antenna or RF module sensitivity. This section explains some layout recommendations for the M2.COM board.

1. High speed signals (ex: USB 2.0, CAN Bus, SDIO and SPI etc.) should not be routed near the antenna.
2. Reserve a RC filter to the signal-ended CLK signals near the receiver side to optimize signal integrity.
3. The routing of high speed signals should not be bent 90 degrees.
4. High speed signals should not be routed around the edge of the PCB to reduce fringing effects.
5. The routing of high speed signals should follow the 3W rule; for instance, if the width of a high speed signal is W, keep 3W distance between the high speed signal and other traces to reduce coupling effects.

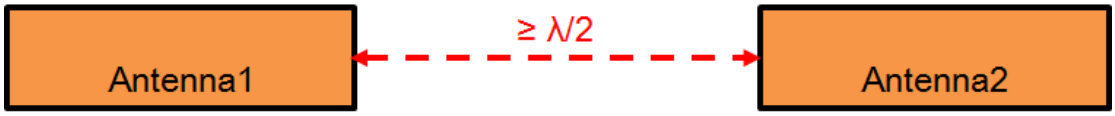
6. Antenna Recommendations

6.1 Antenna Placement

Antenna placement of a wireless system is the first priority of RF system design. Poor antenna placement may cause bad RF performance. In this chapter, the antenna placement suggestions are as follows.

1. The antenna should be placed on the edge or corner of the PCB.
2. Make sure antenna impedance is 50ohm matching. The antenna impedance can be measured by a network analyzer.
3. Do not place any metal or magnetic material near the antenna that might decrease antenna performance. The suggested distance between metal/magnet material and antenna is 5 mm or more.
4. An omni-directional antenna is suggested to transmit and receive RF signals.
5. If the wireless system has two or more antennas, the suggested distance between them should be longer than $\lambda/2$ to enhance isolation. For example, the wavelength of 2.4GHz signal is 125 mm. Thus the distance between two 2.4GHz antennas should be greater than $\lambda/2$ = 62.5mm. Isolation should be 20dB.

Figure 24 Suggested distance between two antennas



6. If the antenna is a printed PIFA or monopole type antenna, maintaining sufficient dimensions of antenna ground is important to performance. The suggested antenna ground dimension can be found with your antenna supplier. Or verify it with Network Analyzer.
7. Antenna must be far from noise sources as high speed digital IC, Switching Power Supply (Power IC), and noisy power chokes can produce harmonic frequencies that interfere with RF performance and sensitivity.

6.2 Antenna Routings

This section provides good practices in antenna cable routing.

1. Make sure no other cables are routed near the antenna(s). Close cables may reduce antenna performance and produce noise issues.
2. Antenna cables must not go through PCB high speed (e.g.: USB 2.0, CAN Bus, SDIO, SPI, etc.) and power choke regions.
3. Antenna cables should be as short as possible to avoiding cable loss issues. Cable length should be shorter than 700mm.
4. Antenna cables should not be sharply bent; sharp bends affect cable impedance.

7. GPIO

7.1 M2.COM Module GPIO

M2.COM Modules support 16 general purpose IO pins: GPIO0 to GPIO15. Each of these can be configured as an input or output pin. GPIO0 to GPIO7 are output defaults. GPIO8 to GPIO9 are multi-function pins that define PWM or GPIO. GPIO10 to GPIO15 are multi-function pins that define ADC or GPIO. The M2.COM specification recommends the use of GPIO0 to GPIO7 as I/O and the use of GPIO8 to GPIO9 as outputs. The other 6 GPIOs (GPIO10 to GPIO15) are Inputs and analog. GPIO voltage level is 3.3V.

7.2 M2.COM GPIO Multi-function Pins

Table 2 Summary of GPIO pin grouping

Signal name	Pin Type	Pwr Rail / Tolerance	Description
GPIO0~7	I/O	3.3V / 3.3V	General purpose input / output 0~7
	CMOS		Default setting is GPO
PWM0~1 / GPIO8~9	O	3.3V / 3.3V	Pulse Width Modulation for Customer used
			Default setting is 100KHz
	CMOS		Multi-Function with GPIO8~9
ADC0~3 / GPIO10~13	I	0~3.3V	Analog-to-Digital Converter for Customer used
	Analog		Multi-Function with GPIO10~15
ADC4 / GPIO14	I	0~3.3V	Analog-to-Digital Converter for Customer used
			Default use to detect VCC power voltage
	Analog		Multi-Function with GPIO14
ADC5 / GPIO15	I	0~3.3V	Analog-to-Digital Converter for Customer used
			Default use to detect USB OTG VBUS voltage
	Analog		Multi-Function with GPIO15

8. Thermal Design and Management

8.1 General

M2.COM Modules generally have less power dissipations that use the MCU for ARM based designs. Most applications with M2.COM modules are integrated sensor devices. The applications may be used as sensor devices for temperature sensing. You may consider calibrating room temperature and module power dissipations to influence sensor operation. No specific maximum dissipation limits are given.

8.2 Thermal Design Power

Establish dissipation responses of modules and systems for Thermal Design Power. Break down the system level environment (various categories defined; many assumptions) and M2.COM card component type (generic packages, power maps defined) of TDP that will be considered thermal solution and calibration that should be considered the steady state dissipation and peak state dissipation. Need to make sure to meet Die maximum temperature first and review temperature influence on sensor operation. The Thermal Dissipation estimate of the Wi-Fi module is around 2 watts, and that may deviate with each ASIC vendor. Please refer to module specs and your solutions.

9. Carrier Board PCB Design Overview

9.1 General PCB Stack-up and Consideration

This section presents an example stack-up for a carrier board based on the M2.COM Module form factor.

***Note**: If the guidelines are followed, measure impedance and critical signals to ensure proper signal integrity and flight timing.*

9.2 PCB Stack-up

A platform based on the M2.COM Module requires a board stack-up yielding a target nominal impedance for differential signals and single-ended signals. The platform should also target the trace widths and spacing to meet the routing specifications shown in Tables 3 and 4. The stack-up numbers may vary due to PCB material differences and type, thus it is important to work with your PCB vendors to fine tune specific impedance tolerances. Please refer to the 4-layer board stack-up in Figure 24 and Table 3; 6-layer board stack-up in Figure 25 and Table 4.

Figure 25 Four Layer PCB Stack-Up Example of 1.5mm (58 mils) Thick PCB

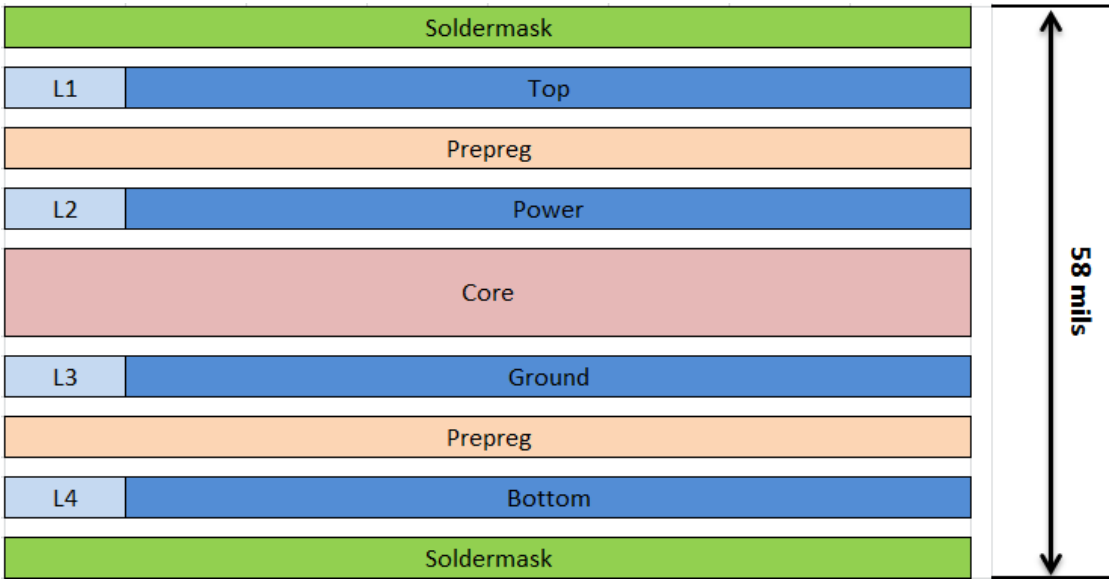
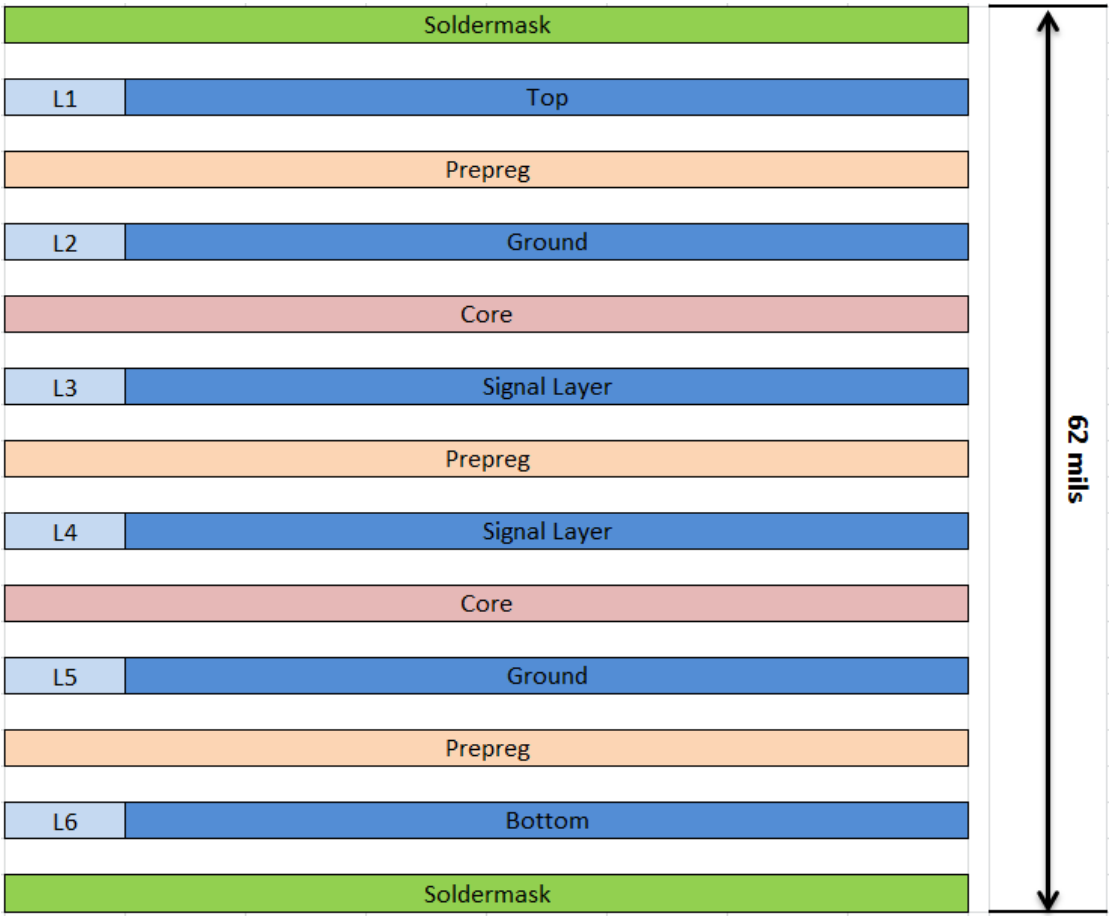


Figure 26 Six Layer PCB Stack-Up Example of 1.5mm (58 mils) Thick PCB



9.3 Trace Parameters for Single End and High Speed Differential Interface

Table 3 4-Layer Impedance and Trace Width/Spacing of 1.5 mm (58 mil) thick PCB

Layer	Description	1.6mm Thick PCB (In Mils)	Comments	Single End 50 ohms Trace Width	Differential 90 ohms Trace Width/Spacing	Differential 100 ohms Trace Width/Spacing
	Soldermask	0.6				
L1	Top	1.5	0.5 oz (Cu weight) + Plating	5 mils	4.5/6 mils	4/9 mils
	Prepreg	3.3	Depends on PCB vender			
L2	Ground	1.3	1 oz (Cu Weight)			
	Core	44.6	4 mil Core			
L3	Ground	1.3	1 oz (Cu Weight)			
	Prepreg	3.3	Depends on PCB vender			
L4	Bottom	1.5	0.5 oz (Cu weight) + Plating	5 mils	4.5/6 mils	4/9 mils
	Soldermask	0.6				
Finished		58 mils				

Table 4 6-Layer Impedance and Trace Width/Spacing of 1.6 mm (62 mil) thick PCB

Layer	Description	1.6mm Thick PCB (In Mils)	Comments	Single End 50 ohms Trace Width	Single End 55 ohms Trace Width	Differential 90 ohms Trace Width/Spacing	Differential 100 ohms Trace Width/Spacing
	Soldermask	0.6					
L1	Top	1.5	0.5 oz (Cu weight) + Plating	5 mils	4 mils	5/7 mils	4/10 mils
	Prepreg	3	Depends on PCB vender				
L2	Ground	1.3	1 oz (Cu Weight)				
	Core	4	4 mil Core				
L3	Signal	1.3	1 oz (Cu Weight)	5 mils	4 mils	4.5/8 mils	4/12 mils
	Prepreg	39	Depends on PCB vender				
L4	Power	1.3	1 oz (Cu Weight)				
	Core	4	4 mil Core				
L5	Ground	1.3	1 oz (Cu Weight)				
	Prepreg	3	Depends on PCB vender				
L6	Bottom	1.5	0.5 oz (Cu weight) + Plating	5 mils	4 mils	5/7 mils	4/10 mils
	Soldermask	0.6					
Finished		62.4 mils					