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Product Warranty (2 years)

Advantech warrants to you, the original purchaser, that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products which have been repaired or altered by persons other than repair personnel authorized by Advantech, or which have been subject to misuse, abuse, accident or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech’s high quality-control standards and rigorous testing, most of our customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced at no charge during the warranty period. For out-of-warranty repairs, you will be billed according to the cost of replacement materials, service time and freight. Please consult your dealer for more details.

If you think you have a defective product, follow these steps:

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages you get when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain an RMA (return merchandise authorization) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a fully-completed Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.
5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.
Declaration of Conformity

CE

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from Advantech. Please contact your local supplier for ordering information.

FCC Class B

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.
Technical Support and Assistance

1. Visit the Advantech web site at http://support.advantech.com where you can find the latest information about the product.

2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before you call:
   – Product name and serial number
   – Description of your peripheral attachments
   – Description of your software (operating system, version, application software, etc.)
   – A complete description of the problem
   – The exact wording of any error messages

Warnings, Cautions and Notes

**Warning!**  *Warnings indicate conditions, which if not observed, can cause personal injury!*

**Caution!**  *Cautions are included to help you avoid damaging hardware or losing data. e.g.*

*There is a danger of a new battery exploding if it is incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.*

**Note!**  *Notes provide optional additional information.*
Safety Instructions

1. Read these safety instructions carefully.
3. Disconnect this equipment from any AC outlet before cleaning. Use a damp cloth. Do not use liquid or spray detergents for cleaning.
4. For plug-in equipment, the power outlet socket must be located near the equipment and must be easily accessible.
5. Keep this equipment away from humidity.
6. Put this equipment on a reliable surface during installation. Dropping it or letting it fall may cause damage.
7. The openings on the enclosure are for air convection. Protect the equipment from overheating. DO NOT COVER THE OPENINGS.
8. Make sure the voltage of the power source is correct before connecting the equipment to the power outlet.
9. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
10. All cautions and warnings on the equipment should be noted.
11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage by transient overvoltage.
12. Never pour any liquid into an opening. This may cause fire or electrical shock.
13. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.
14. If one of the following situations arises, get the equipment checked by service personnel:
   - The power cord or plug is damaged.
   - Liquid has penetrated into the equipment.
   - The equipment has been exposed to moisture.
   - The equipment does not work well, or you cannot get it to work according to the user's manual.
   - The equipment has been dropped and damaged.
   - The equipment has obvious signs of breakage.
15. DO NOT LEAVE THIS EQUIPMENT IN AN ENVIRONMENT WHERE THE STORAGE TEMPERATURE MAY GO BELOW -20° C (-4° F) OR ABOVE 60° C (140° F). THIS COULD DAMAGE THE EQUIPMENT. THE EQUIPMENT SHOULD BE IN A CONTROLLED ENVIRONMENT.
16. CAUTION: DANGER OF EXPLOSION IF BATTERY IS INCORRECTLY REPLACED. REPLACE ONLY WITH THE SAME OR EQUIVALENT TYPE RECOMMENDED BY THE MANUFACTURER, DISCARD USED BATTERIES ACCORDING TO THE MANUFACTURER'S INSTRUCTIONS.

The sound pressure level at the operator's position according to IEC 704-1:1982 is no more than 70 dB (A).

DISCLAIMER: This set of instructions is given according to IEC 704-1. Advantech disclaims all responsibility for the accuracy of any statements contained herein.
Safety Precaution - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electrical shock, always disconnect the power from your PC chassis before you work on it. Don't touch any components on the CPU card or other cards while the PC is on.
- Disconnect power before making any configuration changes. The sudden rush of power as you connect a jumper or install a card may damage sensitive electronic components.
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Appendix D Register of PCI-1751

D.1 Register Format of PCI-1751
Chapter 1

General Information
1.1 Introduction

The PCI-1751 is a 48-bit DI/O and counter/timer card with PCI bus. It provides you with 48 bits of parallel digital input/output as well as 3 timers. It emulates mode 0 of the 8255 PPI chip, but the buffered circuits offer a higher driving capability than the 8255.

The card emulates two 8255 PPI chips to provide 48 DI/O bits. The I/O bits are divided into six 8-bit I/O ports: A0, B0, C0, A1, B1 and C1. You can configure each port as either input or output via software.

The dual interrupt handling capability provides users the flexibility to generate interrupts to a PC. A pin in the connector can output a digital signal simultaneously with the card’s generating an interrupt. This card uses a high density SCSI 68-pin connector for easy and reliable connections to field devices.

Two other features give the PCI-1751 practical advantages in an industrial setting. When the system is hot reset (the power is not turned off) the PCI-1751 retains the last I/O port settings and output values if the user has set jumper JP4 to enable this feature. Otherwise, port settings and output values reset to their safe default state, or to the state determined by other jumper settings. The PCI-1751’s other useful feature is it supports both wet and dry contacts, allowing it to interface with other devices more easily.

1.1.1 Numbering Convention

All numbers given in this manual are in decimal format unless specifically noted otherwise. In particular, where a register address is given as (Base + 32), the decimal number “32” should be added to the base value.

1.2 Features

- 48 TTL level digital I/O lines.
- Emulates mode 0 of 8255 PPI
- Buffered circuits provide higher driving capability
- Interrupt handling
- Interrupt output pin for simultaneously triggering external devices with the interrupt
- High density SCSI 68-pin connector
- Output status readback
- Two 16-bit timers can be cascaded to one 32-bit timer, and can generate watchdog timer interrupts
- One 16-bit event counter can generate event interrupts
- Keeps port I/O settings and digital output states after hot system reset
- Supports dry contact and wet contact

1.3 Applications

- Industrial AC/DC I/O devices monitoring and control
- Relay and switch monitoring and control
- Parallel data transfer
- Sensing the signals of TTL, DTL, CMOS logic
- Driving indicator LEDs
1.4 Installation Guide

Before you install your PCI-1751 card, please make sure you have the following necessary components:
- PCI-1751 card
- Advantech driver DAQNavi (included in the CD-ROM)
- Wiring cable PCL-10168 (optional)
- Wiring board ADAM-3968 (optional)
- Personal computer or workstation with a PCI-bus slot

Some other optional components are also available for enhanced operation:
- Application software: Advantech Navigator (Utility) offered by DAQNavi software

After you get the necessary components and maybe some of the accessories for enhanced operation of your card, you can then begin the installation procedures.

1.5 Software Overview

Advantech offers device drivers, SDKs, third-party driver support and application software to help fully exploit the functions of your PCI-1751 card. All these software packages are available on the companion DVD-ROM or you can browse Advantech website to get the latest update: http://www.advantech.com/.

1.6 Accessories

Advantech offers a complete set of accessory products to support the PCI-1751 card. These accessories include:

Wiring Cable
The PCL-10168 shielded cable is specially designed for PCI-1751 cards to provide high resistance to noise. To achieve better signal quality, the signal wires are twisted in such a way as to form a "twisted-pair cable", reducing cross-talk and noise from other signal sources. Furthermore, its digital lines are separately sheathed and shielded to neutralize EMI/EMC problems.

Wiring Boards
The ADAM-3968 is a 68-pin D-type wiring terminal module for DIN-rail mounting. This terminal module can be readily connected to the Advantech cards and allow easy yet reliable access to individual pin connections for the PCI-1751 card.
Chapter 2

Installation
2.1 Unpacking

After receiving your PCI-1751 package, please inspect its contents first. The package should contain the following items:

- PCI-1751 card
- Companion CD-ROM (Device Drivers included)
- Startup Manual

The PCI-1751 card harbors certain electronic components vulnerable to electrostatic discharge (ESD). ESD could easily damage the integrated circuits and certain components if preventive measures are not carefully paid attention to.

Before removing the card from the antistatic plastic bag, you should take following precautions to ward off possible ESD damage:

- Touch the metal part of your computer chassis with your hand to discharge static electricity accumulated on your body. Or one can also use a grounding strap.
- Touch the anti-static bag to a metal part of your computer chassis before opening the bag.
- Take hold of the card only by the metal bracket when removing it out of the bag.

After taking out the card, first you should:

Inspect the card for any possible signs of external damage (loose or damaged components, etc.). If the card is visibly damaged, please notify our service department or our local sales representative immediately. Avoid installing a damaged card into your system.

Also pay extra caution to the following aspects to ensure proper installation:

- Avoid physical contact with materials that could hold static electricity such as plastic, vinyl and Styrofoam.
- Whenever you handle the card, grasp it only by its edges. DO NOT TOUCH the exposed metal pins of the connector or the electronic components.

**Note!** Keep the anti-static bag for future use. You might need the original bag to store the card if you have to remove the card from PC or transport it elsewhere.
2.2 Hardware Installation

After the device driver installation is completed, you can now go on to install the PCI-1751 card in any PCI slot on your computer. But it is suggested that you should refer to the computer user manual or related documentation if you have any doubt. Please follow the steps below to install the card on your system.

1. Turn off your computer and unplug the power cord and cables. TURN OFF your computer before installing or removing any components on the computer.
2. Remove the cover of your computer.
3. Remove the slot cover on the back panel of your computer.
4. Touch the metal part on the surface of your computer to neutralize the static electricity that might be on your body.
5. Insert the PCI-1751 card into a PCI slot. Hold the card only by its edges and carefully align it with the slot. Insert the card firmly into place. Use of excessive force must be avoided, otherwise the card might be damaged.
6. Fasten the bracket of the PCI card on the back panel of the computer.
7. Connect appropriate accessories to the PCI card.
8. Replace the cover of your computer chassis. Re-connect the cables you removed in step 2.
9. Plug in the power cord and turn on the computer.

After your card is properly installed on your system, you can now configure your device using the Device Installation Program that has itself already been installed on your system during driver setup. A complete device installation procedure should include device setup, configuration and testing. The following sections will guide you through the Setup, Configuration and Testing of your device.
Chapter 3

Signal Connections
3.1 Overview

Maintaining signal connections is one of the most important factors in ensuring that your application system is sending and receiving data correctly. A good signal connection can avoid unnecessary and costly damage to your PC and other hardware devices. This chapter provides useful information about how to connect input and output signals to the PCI-1751 via the I/O connector.

3.2 Switch and Jumper Settings

We designed the PCI-1751 with ease-of-use in mind. It is a "plug and play" card, i.e. the system BIOS assigns the system resources such as base address and interrupt automatically. There are only two functions with 11 jumpers to be set by the user. The following section describes how to configure the card. You may want to refer to the figure below for help in identifying card components.

![Figure 3.1 Location of connectors and jumpers](image)

Jumper Settings to Set Ports as Input or Output by Software

By shorting the upper two pins of jumpers JPA0, JPB0, JPC0L, JPC0H, JPA1, JPB1, JPC1L or JPC1H, a user sets the corresponding ports to be configurable as input or output ports by software. (JPA0 means jumper for port A0, JPB0 means jumper for port B0, etc.) The initial state of each port after system power on or reset will be set as input logic 1 (voltage high), provided that no external signals are connected, and provided jumper JP4 does not determine otherwise (see Jumper J4 discussion below).

Using Jumpers to Set Ports as Output Ports

By shorting the lower two pins of the jumpers JPA0, JPB0, JPC0L, JPC0H, JPA1, JPB1, JPC1L or JPC1H, a user sets the corresponding ports to be output ports. (JPA0 means jumper for port A0, JPB0 means jumper for port B0, etc.) Shorting the lower two pins of a port's jumper pins disables the port from being software configurable as an input port. The initial state of each of these ports after system power on or
reset will be logic 0 (voltage low), unless jumper JP4 determines otherwise. (See Jumper JP4 below.)

**Jumper JP4 Restores Ports to Their Condition Prior to Reset**

Jumper JP4 gives the PCI-1751 a new and valuable capability. With JP4 enabled, the PCI-1751 "memorizes" all port I/O settings and output values, and, in the event of a "hot" reset, the settings and output values present at the port just prior to reset are restored to each port following reset. This feature applies to both ports set by software, and to ports configured as output ports via jumper. Depending on the application, this capability may allow a card to be reset without requiring a complete shutdown of processes controlled by the card (since port values are left unchanged and are interrupted only momentarily).

Complete loss of power to the chip clears chip memory. Thus, even if JP4 is enabled, if the power to the card is disconnected, the card's initial power-on state will be the default state (for software-set ports) or the state of an output port with voltage low output (for jumper-set ports).

When jumper JP4 is not enabled, power-off or reset results in ports returning to their default state (for software-set ports) or returning to the state of output port with voltage low output (for jumper-set ports).

**Select Clock Source of Timers and Counter**

Jumpers JP1, JP2 and JP3 are used to select the clock source of Timer 0, Timer 1 and Counter 2, respectively. Short the upper two pins of the jumpers to select an external clock source, or short the lower two pins to select an internal clock source. However, the internal clock source of Timer 1 is connected to the output of Timer 0, so shorting the upper two pins of JP2 results in the cascading of Timer 0 and Timer 1 as a 32-bit timer.

<table>
<thead>
<tr>
<th>Table 3.1: Summary of Jumper Settings</th>
</tr>
</thead>
<tbody>
<tr>
<td>Names of Jumpers</td>
</tr>
<tr>
<td>------------------</td>
</tr>
<tr>
<td>JPA0, JPA1: Jumpers for ports A0, A1</td>
</tr>
<tr>
<td>JP0, JPB1: Jumpers for ports B0, B1</td>
</tr>
<tr>
<td>JPC0L, JPC1L: Jumpers for low nibble of ports C0, C1</td>
</tr>
<tr>
<td>JPC0H, JPC1H: Jumpers for high nibble of ports C0, C1</td>
</tr>
<tr>
<td>JP1: Timer 0</td>
</tr>
<tr>
<td>JP2: Timer 1</td>
</tr>
<tr>
<td>JP3: Counter 2</td>
</tr>
<tr>
<td>JP4</td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>
### 3.3 Pin Assignments

**Description of pin use:**
- **PA00 ~ PA07**: I/O pins of Port A0
- **PA10 ~ PA17**: I/O pins of Port A1
- **PB00 ~ PB07**: I/O pins of Port B0
- **PB10 ~ PB17**: I/O pins of Port B1
- **PC00 ~ PC07**: I/O pins of Port C0
- **PC10 ~ PC17**: I/O pins of Port C1
- **CNT0_OUT, CNT1_OUT and CNT2_OUT**: Output pins of Counter/Timer 0, 1 and 2
- **CNT0_CLK, CNT1_CLK and CNT2_CLK**: External clock source of Counter / Timer 0, 1 and 2
- **CNT0_G, CNT1_G and CNT2_G**: Gate control pins of Counter / Timer 0, 1 and 2
- **INT_OUT**: Interrupt output. This pin changes to logic 1 whenever the PCI-1751 generates an interrupt, and returns to logic 0 when the interrupt is cleared.
- **GND**: Ground
- **VCC**: +5 VDC voltage output

<table>
<thead>
<tr>
<th>ID3</th>
<th>ID2</th>
<th>ID1</th>
<th>ID0</th>
<th>Board ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
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<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
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<td>0</td>
<td>1</td>
<td>2</td>
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<td>0</td>
<td>0</td>
<td>3</td>
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<td>1</td>
<td>1</td>
<td>4</td>
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<td>0</td>
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</tr>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>14</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>15</td>
</tr>
</tbody>
</table>

**Note!** On: 1, Off: 0
### 3.4 Digital I/O Ports

#### Introduction
The PCI-1751 emulates two 8255 programmable peripheral interface (PPI) chips in mode 0, but with higher driving capability than a standard 8255 chip. Each of the 8255 chips has 24 programmable I/O pins that are divided into three 8-bit ports. The total 48 DI/O pins from both chips are divided into 6 ports, designated PA0, PB0, PC0, PA1, PB1 and PC1. Each port can be programmed as an input or an output port. The I/O pins in port A0 are designated PA00, PA01, ..., PA07; the pins in port B0 are designated PB00, PB01, ..., PB07, etc. These port names are used both in this manual and in the software library. Refer to Section 2.5, Pin Assignments.

#### 8255 Mode 0
- The basic functions of 8255 mode 0 include:
- Two 8-bit I/O ports - port A (PA) and port B (PB)
- Port C is divided into two nibble-wide (4-bit) I/O ports:- PC upper and PC lower
- Any port can be used for either input or output.
- Output status can be read back.

#### Interrupt Function of the DIO Signals
Two I/O pins (PC00 and PC10) can be used to generate hardware interrupts. A user can program the interrupt control register (Base + 32) to select the interrupt sources. Refer to "Interrupt Function" in this chapter for details about interrupt control.

#### Input/Output Control
A control word can be written to a port's configuration register (Base+3 for port 0 and Base+7 for port 1) to set the port as an input or an output port, unless the ports are set as output ports via jumpers (refer to Section 2.3, Jumper Settings). Table 3-1 shows the format of a control word.

<table>
<thead>
<tr>
<th>Table 3.3: Bit map of Port Configuration Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>D7</td>
</tr>
<tr>
<td>-------</td>
</tr>
<tr>
<td>Don’t care</td>
</tr>
</tbody>
</table>

**Note!** A control word has no effect if the corresponding port is set as an output port by a jumper.

**Warning!** Before setting any port as an output port via software, make sure that a safe output value has also been set. An output voltage will appear at the pins immediately following the control word taking effect. If no output value was specified, the value will be indeterminate (either 0 or 1), which may cause a dangerous condition.
Initial Configuration

The initial configuration of each port depends on the input/output jumper setting of each port, on the setting of the jumper JP4, and on whether the power was actually disconnected or whether the system was hot reset.

If jumper JP4 is not enabled, all ports configured by software are automatically set as input ports during system start up or reset, with a default signal level of logic 1 (high). All ports set via jumpers as output ports are set as output ports during system start up or reset, signal level logic 0 (0 V).

If the jumper JP4 is enabled and the initial configuration is caused by a reset, all ports will return to the states they had just prior to the reset.

The reset must be a "hot" reset (power not disconnected) for enabled JP4 to return ports to their prior values. Otherwise, the card behaves as though JP4 were not enabled. Refer to "Jumper settings" in Chapter 2 for more information.

Dry Contact Support for Digital Input

Each digital input channel accepts either dry contact or 0 ~ 5 VDC wet contact inputs. Dry contact capability allows the channel to respond to changes in external circuitry (e.g., the closing of a switch in the external circuitry) when no voltage is present in the external circuit.

The figure below shows external circuitry with both wet and dry contact components, connected as an input source to one of the card’s digital input channels.

Note! For wet contact configurations, a malfunction may occur if the internal resistance of the voltage source is significant (> 1.5 k Ω). It is advisable to connect a 1.5 k Ω resistor in parallel with such a voltage source to avoid a voltage rise inside the voltage source.
3.5 **Timer/Counter Operation**

**Introduction**

The PCI-1751 includes one 8254 compatible programmable timer/counter chip which provides three 16-bit counters, designated as Timer 0, Timer 1 and Counter 2. Each has 6 operation modes. Timer 0 and Timer 1 can be used separately or can be cascaded to create one 32-bit timer. Both Timer 1 and Counter 2 can generate interrupts to the computer. Please refer to Appendix A for more information on the operation modes of the counter chip. The block diagram of the timer/counter system is shown in figure below.

**Timer 0 & 1:**

Two 16-bit Timers or One 32-bit Timer. Timer 0 and Timer 1 of the counter chip can be used separately or can be cascaded to create a 32-bit programmable timer by setting jumper JP2. By setting the clock source of Timer 1 to be an external source, you can use Timer 0 and Timer 1 as two separate 16-bit timers. By setting the clock source of Timer 1 to be the output of Timer 0 (internal source) these two timers are cascaded to become one 32-bit timer. Setting jumper JP1 sets the clock source of Timer 0 to be external, and this allows Timer 0 and Timer 1 to be cascaded into a 32-bit event counter.

**Counter 2:**

Counter 2 can be a 16-bit timer or an event counter, selectable by setting JP3. When the clock source is set for an internal source, Counter 2 is a 16-bit timer; when set as an external source, then Counter 2 is an event counter. Counter 2 is set as mode 0 (interrupt on terminal count) in the driver provided by Advantech.

**Timer/Counter Frequency and Interrupt:**

The input clock frequency of the counter/timers is 10 MHz. The output of both Timer 1 and Counter 2 can generate interrupts for the system (refer to section 3.3). The maximum and minimum timer interrupt frequency is \((10 \text{ MHz})/(2)=(5 \text{ MHz})\) and \((10 \text{ MHz})/((65535*65535))=0.002328 \text{ Hz}\), respectively.
The gates of the counter/timers are internally pulled to +5 V when gate control is enabled, but a user can also set it using the connector pins (CNT0_G, CNT1_G and CNT2_G).

3.6 Interrupt Function

Introduction
Two lines in each I/O port (C0 and C4) and two of the three counter outputs (Timer 1 and Counter 2) are connected to the interrupt circuitry. The "Interrupt Control Register" of the PCI-1751 controls how the combination of the 6 signals generates an interrupt. Two interrupt request signals can be generated at the same time, and then the software can service these two request signals by ISR. The dual interrupt sources provide the card with more capability and flexibility.

IRQ Level
The IRQ level is set automatically by the PCI plug and play BIOS and is saved in the PCI controller. There is no need for users to set the IRQ level. Only one IRQ level is used by this card, although it has two interrupt sources.

Interrupt Control Register (Base + 32)
The "Interrupt Control Register" (Base + 32) controls the interrupt signal source, edge and flag. Table 3-2 shows the bit map of the interrupt control register. The register is a readable/writable register.

When writing to it, it is used as a control register, and when reading from it, it is used as a status register.

M00 and M01: "mode bits" of port 0
M10 and M11: "mode bits" of port 1
E0, E1: triggering edge control bits
F0, F1: flag bits

Interrupt Source Control
The "mode bits" in the interrupt control register determine the allowable sources of signals generating an interrupt. Bit 0 and bit 1 determine the interrupt source for port 0, and bit 4 and bit 5 determine the interrupt source for port 1, as indicated in Figure below. Table 3.4 shows the relationship between an interrupt source and the values in the mode bits.

<table>
<thead>
<tr>
<th>Port #</th>
<th>Port1</th>
<th>Port 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit #</td>
<td>D7</td>
<td>D6</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>F1</td>
<td>E1</td>
</tr>
</tbody>
</table>

M00 and M01: "mode bits" of port 0
M10 and M11: "mode bits" of port 1
E0, E1: triggering edge control bits
F0, F1: flag bits
Chapter 3 Signal Connections

Interrupt Triggering Edge Control

The interrupt can be triggered by a rising edge or a falling edge of the interrupt signal, selectable by the value written in the "triggering edge control" bit in the interrupt control register, as shown in Table 3.6.

<table>
<thead>
<tr>
<th>E0 or E1</th>
<th>Triggering edge of interrupt signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Rising edge trigger</td>
</tr>
<tr>
<td>0</td>
<td>Falling edge trigger</td>
</tr>
</tbody>
</table>

Interrupt Flag Bit

The "interrupt flag" bit is a flag indicating the status of an interrupt. It is a readable and writable bit. Read the bit value to find the status of the interrupt, write "1" to this bit to clear the interrupt. This bit must be cleared in the ISR to service the next incoming interrupt.

<table>
<thead>
<tr>
<th>F0 &amp; F1</th>
<th>Interrupt status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read 1</td>
<td>Interrupt exists</td>
</tr>
<tr>
<td>0</td>
<td>No interrupt</td>
</tr>
<tr>
<td>Write 1</td>
<td>Clear interrupt</td>
</tr>
<tr>
<td>0</td>
<td>Don’t care</td>
</tr>
</tbody>
</table>
Appendix A

Specifications
## A.1 PCI-1751 Specifications

### Table A.1: Digital Input

<table>
<thead>
<tr>
<th>Description</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Input Channel</td>
<td>48 (Shared with output)</td>
</tr>
<tr>
<td>Compatibility</td>
<td>5 V/TTL</td>
</tr>
<tr>
<td>Interrupt Inputs</td>
<td>2 (PC00,PC10)</td>
</tr>
</tbody>
</table>
| Input Voltage        | Logic 0: 0.8 V (max.)  
                      | Logic 1: 2 V (min.)   |

### Table A.2: Digital Output

<table>
<thead>
<tr>
<th>Description</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Output Channel</td>
<td>48 (Shared with input)</td>
</tr>
<tr>
<td>Compatibility</td>
<td>5 V/TTL</td>
</tr>
</tbody>
</table>
| Output Voltage       | Logic 0: 0.8 V max. @+24 mA (sink)  
                      | Logic 1: 2 V min. @-15 mA (source) |

### Table A.3: Counter / Timer

<table>
<thead>
<tr>
<th>Description</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channels</td>
<td>3 channels are free for user application</td>
</tr>
<tr>
<td>Compatibility</td>
<td>5 V/TTL</td>
</tr>
<tr>
<td>Resolution</td>
<td>16-bit</td>
</tr>
</tbody>
</table>
| Base Clock           | Channel 0: Internal 10MHz  
                      | External Clock (up to 10MHz)  
                      | Channel 1: Takes input from output of Channel 0  
                      | External Clock (up to 10MHz)  
                      | Channel 2: Internal 10MHz  
                      | External Clock (up to 10MHz)  |
| Max. Input Frequency | 10M Hz              |
| Clock Input          | Logic 0: 0.8 V (max.)  
                      | Logic 1: 2 V (min.)   |
| Gate Input           | Logic 0: 0.8 V (max.)  
                      | Logic 1: 2 V (min.)   |
| Counter Output       | Logic 0: 0.8 V max. @+24 mA (sink)  
                      | Logic 1: 2 V min. @-15 mA (source) |

### Table A.4: General Specifications

<table>
<thead>
<tr>
<th>Description</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O Connector Type</td>
<td>68-pin SCSI-II female</td>
</tr>
<tr>
<td>Dimensions</td>
<td>170 mm x 100 mm (6.9&quot; x 3.9&quot;)</td>
</tr>
</tbody>
</table>
| Power Consumption    | +5V @ 850 mA (typical)  
                      | +5V @ 1 A (max.)       |
| Temperature          | Operating: 0 ~ +70°C (32 ~ 158°F)  
                      | Storage: -20 ~ +80°C (-4 ~ 176°F) |
| Relative Humidity    | 5 ~ 95 % RH non-condensing (refer to IEC 60068-2-3) |
| Certifications       | CE / FCC            |
B.1 PCI-1751 Block Diagram

![PCI-1751 Block Diagram](image)
Appendix C

Function of 8254 Counter Chip
C.1 The Intel 8254

The PCI-1751 uses the Intel 8254 compatible programmable interval timer/counter. The popular 8254 offers three independent 16-bit down counters. Each counter has a clock input, control gate and an output. You can program each counter for maximum count values from 2 to 65535.

The 8254 has a maximum input clock frequency of 10 MHz. The PCI-1751 provides 10 MHz input frequencies to the counter chip from an on-board crystal oscillator.

On the PCI-1751, the 8254 chip's Timer 0 and Timer 1 can be used separately or can be cascaded to create a 32-bit programmable timer by setting JP2. When the clock source of Timer 1 is from an external source, you can use Timer 0 and Timer 1 as two independent 16-bit timers. When the clock source of Timer 1 is set to be the output of Timer 0 (internal source) the two timers are cascaded as a 32-bit timer. When the clock source of Timer 0 is provided externally by setting JP1, Timers 0 and 1 can be used as a 32-bit event counter. Refer to section 2.3.3 for details of jumper settings.

C.2 Counter Read/Write and Control Registers

The 8254 programmable interval timer uses four registers at addresses BASE+24, BASE+25, BASE+26 and BASE+27 for read, write and control of counter functions. Register functions appear below:

<table>
<thead>
<tr>
<th>Register</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>BASE+24</td>
<td>Counter 0 read/write</td>
</tr>
<tr>
<td>BASE+25</td>
<td>Counter 1 read/write</td>
</tr>
<tr>
<td>BASE+26</td>
<td>Counter 2 read/write</td>
</tr>
<tr>
<td>BASE+27</td>
<td>Counter control word</td>
</tr>
</tbody>
</table>

Since the 8254 counter uses a 16-bit structure, each section of read/write data is split into a least significant byte (LSB) and most significant byte (MSB). To avoid errors it is important that you make read/write operations in pairs and keep track of the byte order.

The data format for the control register appears below:

<table>
<thead>
<tr>
<th>BASE+27</th>
<th>8254 control, standard mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit</td>
<td>D7</td>
</tr>
<tr>
<td>Value</td>
<td>SC1</td>
</tr>
</tbody>
</table>

Description:
SC1 & SC0 Select counter

<table>
<thead>
<tr>
<th>Counter</th>
<th>SC1</th>
<th>SC0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Read-back command</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
Appendix C Function of 8254 Counter Chip

RW1 & RW0  Select read/write operation

<table>
<thead>
<tr>
<th>Operation</th>
<th>RW1</th>
<th>RW0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Counter latch</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Read/write LSB</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Read/write MSB</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Read/write LSB first, then MSB</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

M2, M1 & M0  Select operating mode

<table>
<thead>
<tr>
<th>M2</th>
<th>M1</th>
<th>M0</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0 programmable one shot</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1 programmable one shot</td>
</tr>
<tr>
<td>X</td>
<td>1</td>
<td>0</td>
<td>2 Rate generator</td>
</tr>
<tr>
<td>X</td>
<td>1</td>
<td>1</td>
<td>3 Square wave rate generator</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>4 Software triggered strobe</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>5 Hardware triggered strobe</td>
</tr>
</tbody>
</table>

BCD  Select binary or BCD counting

<table>
<thead>
<tr>
<th>BCD</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Binary counting 16-bits</td>
</tr>
<tr>
<td>1</td>
<td>Binary coded decimal (BCD) counting</td>
</tr>
</tbody>
</table>

If you set the module for binary counting, the count can be any number from 0 up to 65535. If you set it for BCD (Binary Coded Decimal) counting, the count can be any number from 0 to 9999.

If you set both SC1 and SC0 bits to 1, the counter control register is in read-back command mode. The control register data format then becomes:

<table>
<thead>
<tr>
<th>BASE+27 8254 control, read-back mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit</td>
</tr>
<tr>
<td>Value</td>
</tr>
</tbody>
</table>

CNT = 0  Latch count of selected counter(s).
STA = 0  Latch status of selected counter(s).
C2, C1 & C0  Select counter for a read-back operation.
    C2 = 1  select Counter 2
    C1 = 1  select Counter 1
    C0 = 1  select Counter 0

If you set both SC1 and SC0 to 1 and STA to 0, the register selected by C2 to C0 contains a byte which shows the status of the counter. The data format of the counter read/write register then becomes:
OUT Current state of counter output
NC Null count is 1 when the last count written to the counter register has been loaded into the counting element

C.3 Counter Operating Modes

C.3.1 MODE 0 - Stop on Terminal Count

The output will be initially low after you set this mode of operation. After you load the count into the selected count register, the output will remain low and the counter will count. When the counter reaches the terminal count, its output will go high and remain high until you reload it with the mode or a new count value. The counter continues to decrement after it reaches the terminal count. Rewriting a counter register during counting has the following results:
1. Writing to the first byte stops the current counting.
2. Writing to the second byte starts the new count.

C.3.2 MODE 1 - Programmable One-shot

The output is initially high. The output will go low on the count following the rising edge of the gate input. It will then go high on the terminal count. If you load a new count value while the output is low, the new value will not affect the duration of the one-shot pulse until the succeeding trigger. You can read the current count at any time without affecting the one-shot pulse. The one-shot is retriggerable, thus the output will remain low for the full count after any rising edge at the gate input.

C.3.3 MODE 2 - Rate Generator

The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the counter register. If you reload the counter register between output pulses, the present period will not be affected, but the subsequent period will reflect the value.

The gate input, when low, will force the output high. When the gate input goes high, the counter will start from the initial count. You can thus use the gate input to synchronize the counter.

With this mode the output will remain high until you load the count register is loaded. You can also synchronize the output by software.

C.3.4 MODE 3 - Square Wave Generator

This mode is similar to Mode 2, except that the output will remain high until one half of the count has been completed (for even numbers), and will go low for the other half of the count. This is accomplished by decreasing the counter by two on the falling edge of each clock pulse. When the counter reaches the terminal count, the state of the output is changed, the counter is reloaded with the full count and the whole process is repeated.
If the count is odd and the output is high, the first clock pulse (after the count is loaded) decrements the count by 1. Subsequent clock pulses decrement the count by 2. After time-out, the output goes low and the full count is reloaded. The first clock pulse (following the reload) decrements the counter by 3. Subsequent clock pulses decrement the count by two until time-out, then the whole process is repeated. In this way, if the count is odd, the output will be high for \((N+1)/2\) counts and low for \((N-1)/2\) counts.

C.3.5 **MODE 4 - Software Triggered Strobe**

After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period then go high again.

If you reload the count register during counting, the new count will be loaded on the next CLK pulse. The count will be inhibited while the GATE input is low.

C.3.6 **MODE 5 - Hardware Triggered Strobe**

The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable.

C.4 **Counter Operations**

C.4.1 **Read/Write Operation**

Before you write the initial count to each counter, you must first specify the read/write operation type, operating mode and counter type in the control byte and write the control byte to the control register (BASE+27).

Since the control byte register and all three counter read/write registers have separate addresses and each control byte specifies the counter it applies to (by SC1 and SC0), no instructions on the operating sequence are required. Any programming sequence following the 8254 convention is acceptable.

There are three types of counter operation: read/load LSB, read/load MSB and read/load LSB followed by MSB. It is important that you make your read/write operations in pairs and keep track of the byte order.

C.4.2 **Counter Read-back Command**

The 8254 counter read-back command lets you check the count value, programmed mode and current states of the OUT pin and Null Count flag of the selected counter(s). You write this command to the control word register. The format is as shown at the beginning of this section.

The read-back command can latch multiple counter output latches. Simply set the CNT bit to 0 and select the desired counter(s). This single command is functionally equivalent to multiple counter latch commands, one for each counter latched.

The read-back command can also latch status information for selected counter(s) by setting STA bit = 0. The status must be latched to be read; the status of a counter is accessed by a read from that counter. The counter status format appears at the beginning of the chapter.
C.4.3 Counter Latch Operation

Users often want to read the value of a counter without disturbing the count in progress. You do this by latching the count value for the specific counter then reading the value.

The 8254 supports the counter latch operation in two ways. The first way is to set bits RW1 and RW0 to 0. This latches the count of the selected counter in a 16-bit hold register. The second way is to perform a latch operation under the read-back command. Set bits SC1 and SC0 to 1 and CNT = 0. The second method has the advantage of operating several counters at the same time. A subsequent read operation on the selected counter will retrieve the latched value.

C.5 Counter Applications

The 8254 compatible programmable interval timer/counter on your PCI-1751 interface card is a very useful device. You can program timers 1 and 2 to serve as timers, event counters, square wave generators, or as a watchdog to generate regular interrupts at a fixed interval.
D.1 **Register Format of PCI-1751**

<table>
<thead>
<tr>
<th>Base Address + (Decimal)</th>
<th>Function</th>
<th>Read</th>
<th>Write</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Port A0</td>
<td>Port A0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Port B0</td>
<td>Port B0</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Port C0</td>
<td>Port C0</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
<td>Port 0 Configuration</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Port A1</td>
<td>Port A1</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Port B1</td>
<td>Port B1</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Port C1</td>
<td>Port C1</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Reserved</td>
<td>Port 1 Configuration</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>B0ID[3:0]</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>9–23</td>
<td>Reserved</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>8254 Counter 0</td>
<td>8254 Counter 0</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>8254 Counter 1</td>
<td>8254 Counter 1</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>8254 Counter 2</td>
<td>8254 Counter 2</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>Reserved</td>
<td>8254 Control Register</td>
<td></td>
</tr>
<tr>
<td>28–31</td>
<td>Reserved</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>Interrupt Status Register</td>
<td>Interrupt Status Register</td>
<td></td>
</tr>
</tbody>
</table>