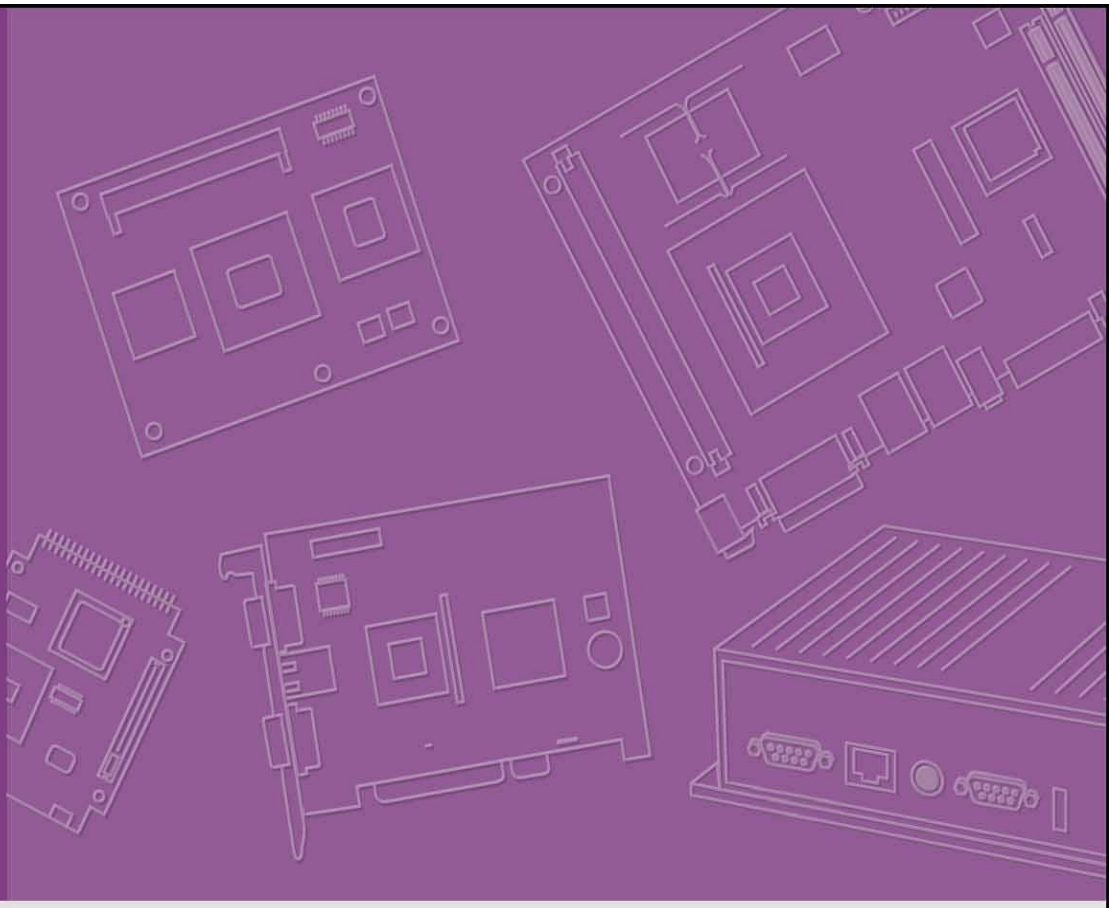
Embedded - IoT



CarrierBoard Design Guide

COM Express®

SOM-7569 COMe TYPE10

R160 2019'10'25

ADVANTECH

Enabling an Intelligent Planet

Contents

1. Introduction 7
1.1 About This Document 7
1.2 Signal Table Terminology 7
1.3 Terminology 8
1.4 Reference Documents 12
1.5 Revision History 12
1.6 SOM-7569 Block Diagram 13
2 COM Express Type 10 Interfaces 14
2.1 COM Express Type 10 Connector Layout 14
2.2 COM Express Type 10 Connector Pin-out 15
2.3 PCI Express 19
2.3.1 COM Express A-B Connector PCIe Groups 19
2.3.2 General Purpose PCIe Signal Definitions 19
2.3.3 PCI Express Lane Configurations – Per COM Express Spec 22
2.3.4 PCI Express* General Routing Guidelines 23
2.3.4.1 PCI Express Insertion Loss Budget with Slot Card 23
2.3.4.2 PCI Express Insertion Loss Budget with Carrier Board PCIE Device 25
2.3.4.3 PCI Express Differential Transitional Via Recommendations 27
2.3.5 PCI Express* Trace Length Guidelines 28
2.4 Digital Display Interfaces (DDI) 30
2.4.1 DDI Signal Definitions 30
2.4.2 Digital Display Interfaces (DDI) Routing Guidelines 33
2.4.2.1 DisplayPort Routing Guidelines 33
2.4.2.2 HDMI / DVI Routing Guidelines 35
2.4.3 HDMI / DVI Level Shifter Requirements 37
2.4.4 ESD Protection 37
2.5 LAN Interface 38
2.5.1 LAN Signal Definitions 38
2.5.2 LAN Routing Guidelines 40
2.5.3 LAN Trace Length Guidelines 41
2.5.4 Reference Ground Isolation and Coupling 42
2.6 USB2.0 Ports 43
2.6.1 USB2.0 Signal Definitions 43
2.6.1.1 USB Over-Current Protection (USB_x_y_OC#) 46

2.6.1.2 Powering USB devices during S5 46
2.6.2 USB2.0 Routing Guidelines 47
2.6.2.1 USB 2.0 General Design Considerations and Optimization 48
2.6.2.2 USB 2.0 Port Power Delivery 48
2.6.2.3 USB 2.0 Common Mode Chokes 49
2.6.2.4 EMI / ESD Protection 50
2.6.3 USB2.0 Trace Length Guidelines 51
2.7 USB3.0 52
2.7.1 USB3.0 Signal Definitions 52
2.7.1.1 USB Over-Current Protection (USB_x_y_OC#) 54
2.7.1.2 EMI / ESD Protection 54
2.7.2 USB3.0 Routing Guidelines 55
2.7.2.1 USB3.0 Differential Transitional Via Recommendations 55
2.7.3 USB3.0 Trace Length Guidelines 56
2.8 SATA 57
2.8.1 SATA Signal Definitions 57
2.8.2 SATA Routing Guidelines 59
2.8.2.1 General SATA Routing Guidelines 60
2.8.2.2 SATA Differential Transitional Via Recommendations 60
2.8.3 SATA Trace Length Guidelines 61
2.9 LVDS 62
2.9.1 Signal Definitions 62
2.9.1.1 Display Timing Configuration 64
2.9.1.2 Backlight Control 64
2.9.2 LVDS Routing Guidelines 65
2.9.3 LVDS Trace Length Guidelines 66
2.10 Embedded DisplayPort (eDP) 67
2.10.1 eDP Signal Definitions 67
2.10.2 eDP Trace Length Guidelines 69
2.11 Digital Audio Interfaces 70
2.11.1 Audio Codec Signal Descriptions 70
2.11.2 Audio Routing Guidelines 72
2.11.3 Audio Trace Length Guidelines 73
2.12 LPC Bus – Low Pin Count Interface 74
2.12.1 LPC Signal Definition 74
2.12.2 LPC Routing Guidelines 75
2.12.2.1 General Signals 75

2.12.2.2 Bus Clock Routing 76
2.12.3 LPC Trace Length Guidelines 76
2.13 SPI – Serial Peripheral Interface Bus 77
2.13.1 SPI Signal Definition 77
2.13.2 SPI Routing Guidelines 79
2.13.3 SPI Trace Length Guidelines 79
2.14 General Purpose I2C Bus Interface 80
2.14.1 Signal Definitions 80
2.14.2 I2C Routing Guidelines 81
2.14.3 I2C Trace Length Guidelines 82
2.14.4 Connectivity Considerations 82
2.15 System Management Bus (SMBus) 83
2.15.1 SMB Signal Definitions 84
2.15.2 SMB Routing Guidelines 85
2.15.3 SMB Trace Length Guidelines 85
2.16 General Purpose Serial Interface 86
2.16.1 Serial interface Signal Definitions 86
2.16.2 Serial interface Routing Guidelines 87
2.16.3 Serial interface Trace Length Guidelines 87
2.17 CAN Interface 88
2.17.1 CAN interface Signal Definitions 88
2.17.2 CAN interface Routing Guidelines 88
2.17.3 CAN interface Trace Length Guidelines 89
2.18 Miscellaneous Signals 90
2.18.1 Miscellaneous Signals 90
2.18.1.1 Logic Level Signals on Pins Reclaimed from VCC_12 94
2.18.2 Power Management Signals 95
2.18.3 Thermal Interface 97
2.18.4 Miscellaneous Signals Routing Guidelines 97
2.18.5 SDIO Signals Trace Length Guidelines 98
2.19 Reserved Pins 99
2.19.1 Reserved Pins Definitions 99
3 Power 100
3.1 General Power requirements 100
3.2 VCC5_SBY Routing 100
3.3 ATX and AT Power Sequencing Diagrams 100

3.4 Input Power - Rise Time 103
3.5 Design Considerations for Carrier Boards containing FPGAs/CPLDs.. 104
4 Electrical Characteristics..... 105
4.1 Absolute Maximum Ratings 105
4.2 DC Characteristics 105
4.3 Inrush Current 105

List of Tables

Table 1: Signal Table Terminology Descriptions 7
Table 2: Conventions and Terminology 8
Table 3: COM Express Type 10 Pin-out 15
Table 4: General Purpose PCI Express Signal Descriptions 19
Table 5: Differential Transitional Via Layout Recommendations 27
Table 6: PCI Express* Slot Card / Device Down Trace Length Guidelines 29
Table 7: Port / HDMI / DVI Pin-out of Type 10 30
Table 8: DDI0 Signal Description 31
Table 9: DisplayPort Insertion Loss Budget 33
Table 10: DisplayPort Connector / Device Down Trace Length Guidelines 34
Table 11: HDMI / DVI (TMDS) Insertion Loss Budget 35
Table 12: HDMI / DVI Connector / Device Down Trace Length Guidelines 36
Table 13: LAN Interface Signal Descriptions 38
Table 14: 10/100/1000 Ethernet Insertion Loss Budget, 100 MHz 40
Table 15: Ethernet Trace Length Guidelines 41
Table 16: USB Signal Descriptions 43
Table 17 : USB Insertion Loss Budget, 400 MHz 47
Table 18: USB2.0 Trace Length Guidelines 51
Table 19: USB3.0 Signal Definitions 52
Table 20: USB3.0 Insertion Loss Budget 55
Table 21: USB3.0 Trace Length Guidelines 56
Table 22: SATA Signal Definitions 57
Table 23: SATA Insertion Loss Budge 59
Table 24: SATA Trace Length Guidelines 61
Table 25: LVDS Signal Definitions 62
Table 26: LVDS Trace Length Guidelines 66
Table 27: eDP Signal Definitions 67
Table 28: DisplayPort Connector / Device Down Trace Length Guidelines 69
Table 29: Audio Codec Signal Descriptions 70
Table 30: Audio Trace Length Guidelines 73
Table 31: LPC Interface Signal Definition 74
Table 32: LPC Trace Length Guidelines 76
Table 33: SPI Interface Signal Definition 77
Table 34: Effect of the BIOS disable signals 79

Table 35: SPI Trace Length Guidelines 79
Table 36 35: General Purpose I2C Interface Signal Descriptions 81
Table 37: I2C Trace Length Guidelines 82
Table 38: SMB Signal Definitions 84
Table 39: SMB Trace Length Guidelines 85
Table 40: Serial interface Signal Definitions 86
Table 41: Serial interface Trace Length Guidelines 87
Table 42: CAN interface Signal Definitions 88
Table 43: CAN interface Trace Length Guidelines 89
Table 44: Miscellaneous Signal Definitions 90
Table 45: Signal Definition SDIO 93
Table 46: Power Management Signal Definitions 95
Table 47: Thermal Management Signal Definitions 97
Table 48: SDIO Trace Length Guidelines 98
Table 49: RSVD Definitions 99
Table 50: Power Management Timings 102
Table 51: Absolute Maximum Ratings 105
Table 52: Input Power Consumption of 12V / 4.75V / 20V 105
Table 53: Inrush Current 105

List of Figures

Figure 1: SOM-7569 Block Diagram 13
Figure 2: COM Express Type 10 Connector Layout 14
Figure 3: Differential Transitional Via Layout 27
Figure 4: Topology for PCI Express Slot Card. 28
Figure 5: Topology for PCI Express Device Down. 28
Figure 6: DisplayPort Loss Budget 33
Figure 7: Topology for DisplayPort 34
Figure 8: HDMI / DVI (TMDS) Loss Budget 35
Figure 9: Topology for HDMI / DVI 36
Figure 10: 10/100/1000 Ethernet Insertion Loss Budget 40
Figure 11: Topology for Ethernet Jack 41
Figure 12: USB Insertion Loss Budget 47
Figure 13: USB 2.0 Good Downstream Power Connection 49
Figure 14: USB 2.0 A Common Mode Choke 49
Figure 15: Topology for USB2.0 51
Figure 16: USB3.0 Insertion Loss Budget 55
Figure 17: Topology for USB3.0 56
Figure 18: SATA Insertion Loss Budge 59
Figure 19: Topology for SATA 61
Figure 20: Topology for LVDS 66
Figure 21: Topology for eDP 69
Figure 22: Topology for Audio 73
Figure 23: Topology for LPC 76
Figure 24: Topology for SPI 79
Figure 25: Topology for I2C 82
Figure 26: Topology for SMB 85
Figure 27: Topology for Serial interface 87
Figure 28: Topology for CAN interface 89
Figure 29: Protecting Logic Level Signals on Pins Reclaimed from VCC_12V 94
Figure 30: Topology for SDIO 98
Figure 31: ATX Style Power Up Boot – Controlled by Power Button 101
Figure 32: AT Style Power Up Boot 102

1. Introduction

1.1 About This Document

This design guide provides information for designing a custom system Carrier Board for COM Express Type 10 Module. It includes Signal Descriptions, Routing Guidelines and Trace Length Guidelines. The main purpose is designing Carrier Board for helping customers fast and easy using the module of Advantech to be designed.

1.2 Signal Table Terminology

Table 1 below describes the terminology used in this section for the Signal Description tables.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

The terms "Input" and "Output" and their abbreviations in Table 1 below refer to the Module's view, i.e. an input is an input for the Module and not for the Carrier-Board.

Table 1: Signal Table Terminology Descriptions

Term	*Description*
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3V3_SBY	Bi-directional 3.3V tolerant active during Suspend and running state.
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
OD	Open drain output
P	Power input/output
*_S0	Signal active during running state.
PCIE	In compliance with PCI Express Base Specification
USB	In compliance with the Universal Serial Bus Specification
GbE	In compliance with IEEE 802.3ab 1000BASE-T Gigabit Ethernet
SATA	In compliance with Serial ATA specification
REF	Reference voltage output. May be sourced from a Module power plane.
PDS	Pull-down strap. A Module output pin that is either tied to GND or is not connected. Used to signal Module capabilities (pin-out type) to the Carrier Board.

1.3 Terminology

Table 2: Conventions and Terminology

Terminology	*Description*
AC ‘97 / HDA	Audio CODEC '97/High Definition Audio
ACPI	Advanced Configuration Power Interface – standard to implement power saving modes in PCAT systems
ADD2	Advanced Digital Display, 2nd Generation
ADD2/MEC	Advanced Digital Display, 2nd Generation, Media Expansion Card
Basic Module	COM ExpressR 125mm x 95mm Module form factor.
BIOS	Basic Input Output System – firmware in PC-AT system that is used to initialize system components before handing control over to the operating system.
CAN	Controller-area network (CAN or CAN-bus) is a vehicle bus standard designed to allow microcontrollers to communicate with each other within a vehicle without a host computer.
Carrier Board	An application specific circuit board that accepts a COM ExpressR Module.
Compact Module	COM ExpressR 95mm x 95mm Module form factor
CRT	Cathode Ray Tube
DAC	Digital Analog Converter
DDC	Display Data Control – VESA (Video Electronics Standards Association) standard to allow identification of the capabilities of a VGA monitor
DDI	Digital Display Interface– containing DisplayPort, HDMI/DVI and SDVO
DNI	Do Not Install
DP	DisplayPort is a digital display interface standard put forth by the Video Electronics StandardsAssociation (VESA). It defines a new license free, royalty free, digital audio/videointerconnect, intended to be used primarily between a computer and its display monitor.
DP	DisplayPort is a digital display interface standard put forth by the Video Electronics StandardsAssociation (VESA). It defines a new license free, royalty free, digital audio/videointerconnect, intended to be used primarily between a computer and its display monitor.
DVI	Digital Visual Interface - a Digital Display Working Group (DDWG) standard that defines a standard video interface supporting both digital and analog video signals. The digital signals use TMDS.

Terminology	*Description*
EAPI	Embedded Application Programming Interface Software interface for COM ExpressR specific industrial functions • System information • Watchdog timer • I2C Bus • Flat Panel brightness control • User storage area • GPIO
EDID	Extended Display Identification Data
EDP	Embedded DisplayPort (eDP) is a digital display interface standard produced by the Video Electronics Standards Association (VESA) for digital interconnect of Audio and Video.
EEPROM	Electrically Erasable Programmable Read-Only Memory
EFT	Electrical Fast Transient
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
ExpressCard	A PCMCIA standard built on the latest USB 2.0 and PCI Express buses.
Extended Module	COM ExpressR 155mm x 110mm Module form factor.
FR4	A type of fiber-glass laminate commonly used for printed circuit boards.
Gb	Gigabit
GbE	Gigabit Ethernet
GPI	General Purpose Input
GPIO	General Purpose Input Output
GPO	General Purpose Output
HDA	Intel High Definition Audio (HD Audio) refers to the specification released by Intel in 2004 for delivering high definition audio that is capable of playing back more channels at higher quality than AC97.
HDMI	High Definition Multimedia Interface
I2C	Inter Integrated Circuit – 2 wire (clock and data) signaling scheme allowing communication between integrated circuits, primarily used to read and load register values.
DE	Integrated Device Electronics – parallel interface for hard disk drives – also known as PATA
Legacy Device	Relics from the PC-AT computer that are not in use in contemporary PC systems: primarily the ISA bus, UART-based serial ports, parallel printer ports, PS-2 keyboards, and mice.

	Definitions vary as to what constitutes a legacy device. Some definitions include IDE as a legacy device.

Terminology	*Description*
LAN	Local Area Network
LPC	Low Pin-Count Interface: a low speed interface used for peripheral circuits such as Super I/O controllers, which typically combine legacy-device support into a single IC.
LS	Least Significant
LVDS	Low-Voltage Differential Signaling – widely used as a physical interface for TFT flat panels. LVDS can be used for many high-speed signaling applications. In this document, it refers only to TFT flat-panel applications.
MEC	Media Expansion Card
Mini Module	COM ExpressR 84x55mm Module form factor
MS	Most Significant
NA	Not available
NC	Not connected
OBD-II	On-Board Diagnostics 2nd generation
OEM	Original Equipment Manufacturer
PATA	Parallel AT Attachment – parallel interface standard for hard-disk drives – also known as IDE,AT Attachment, and as ATA
PC-AT	“Personal Computer – Advanced Technology” – an IBM trademark term used to refer to Intel x86 based personal computers in the 1990s
PCB	Printed Circuit Board
PCI	Peripheral Component Interface
PCI Express (PCIe)	Peripheral Component Interface Express – next-generation high speed Serialized I/O bus
PCI Express Lane	One PCI Express Lane is a set of 4 signals that contains two differential lines for Transmitter and two differential lines for Receiver. Clocking information is embedded into the data stream.
PD	Pull Down
PEG	PCI Express Graphics
PHY	Ethernet controller physical layer device
Pin-out Type	A reference to one of seven COM ExpressR definitions for the signals that appear on the COM ExpressR Module connector pins.
PS2 PS2 Keyboard	“Personal System 2” - an IBM trademark term used to refer to Intel x86 based personal computers in the 1990s. The term survives as a reference to

PS2 Mouse	the style of mouse and keyboard interface that were introduced with the PS2 system.

Terminology	*Description*
PU	Pull Up
ROM	Read Only Memory – a legacy term – often the device referred to as a ROM can actually be written to, in a special mode. Such writable ROMs are sometimes called Flash ROMs. BIOS is stored in ROM or Flash ROM.
RTC	Real Time Clock – battery backed circuit in PC-AT systems that keeps system time and dateas well as certain system setup parameters
S0, S1, S2, S3, S4, S5	Sleep States defined by the ACPI specificationS0 Full power, all devices powered S1Sleep State, all context maintained S2 Sleep State, CPU and Cache context lost S3 Suspend to RAM System context stored in RAM; RAM is in standby S4 Suspend to Disk System context stored on disk S5 Soft Off Main power rail off, only standby power rail present
SATA	Serial AT Attachment: serial-interface standard for hard disks
SDVO	Serial Digital Video Out is a proprietary technology introduced by IntelR to add additional video signaling interfaces to a system. Being phased out
SMBus	System Management Bus
SO-DIMM	Small Outline Dual In-line Memory Module
SPI	Serial Peripheral Interface
TBD	To be determined
TMDS	Transition Minimized Differential Signaling - a digital signaling protocol between the graphics subsystem and display. TMDS is used for the DVI digital signals. DC coupled
TPM	Trusted Platform Module, chip to enhance the security features of a computer system.
UIM	User Identity Module
USB	Universal Serial Bus
VESA	Video Electronics Standards Association
WDT	Watch Dog Timer

1.4 Reference Documents

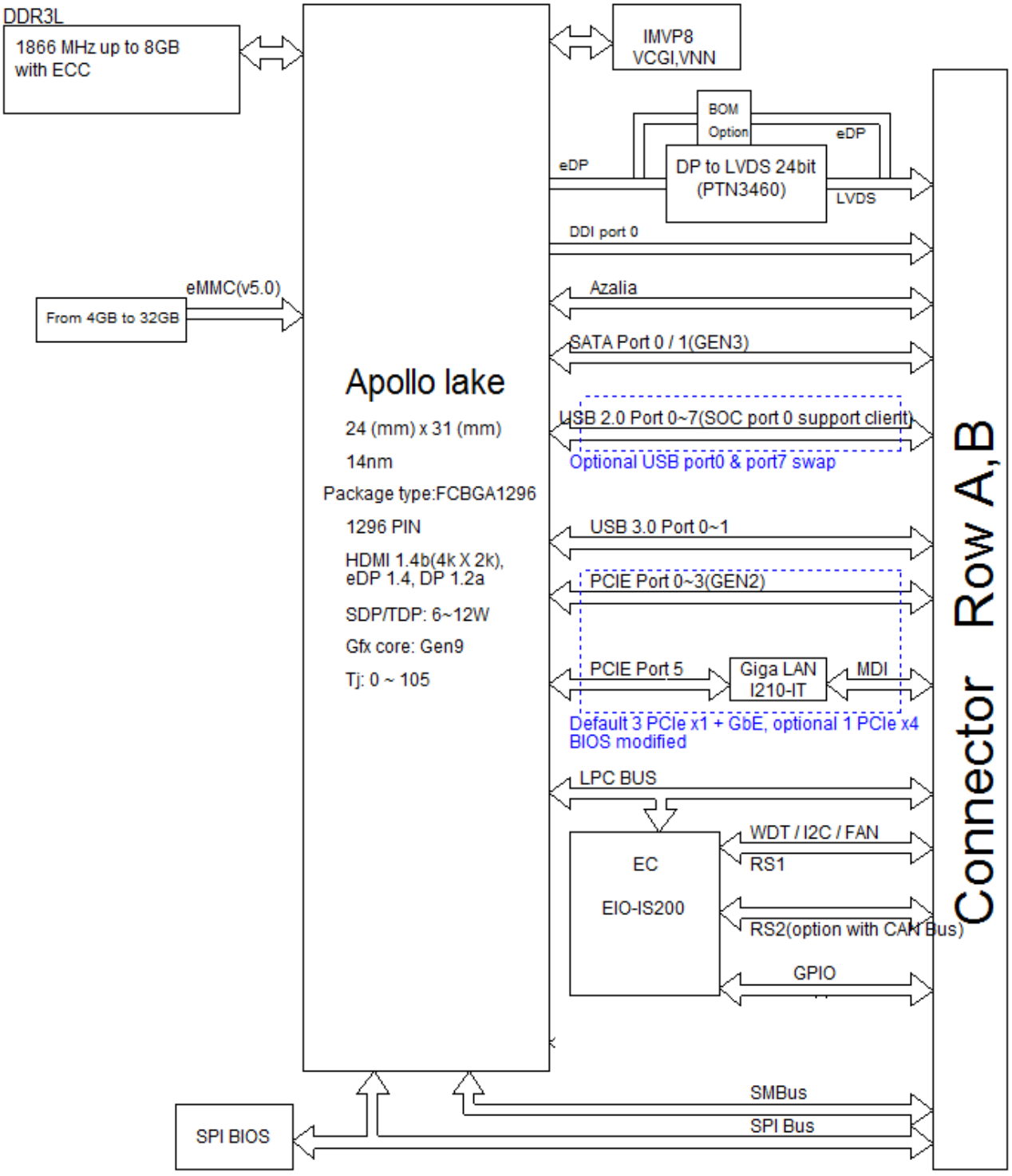
Document
COM Express Carrier Design Guide Rev. 2.0
Intel EDS Document
Intel Layout Guide Document
ATX12V Power Supply Design Guide Rev. 2.01

1.5 Revision History

Revision	Date	PCB Rev.	Changes
0.10	Oct. 06, 2016	A101-2	
0.20	Oct. 27, 2016	A101-2	1. Add eDP Max length. 2. Add SDIO in design guide.
0.30	Nov.02, 2016	A101-2	1. Change eDP Max length form 4” to 10”
0.40	Feb.17, 2017	A101-3	1. No any change for this design guide.
0.50	Apr. 19,2017	A101-4	1. Update Power Consumption. 2. Update USB3.0 mismatch rule. 3. Update SDIO mismatch and trace spacing rule. 4. Update LVDS mismatch rule.
1.00	Jun. 19,2017	A101-5	1. Remove SDIO function.
1.10	Feb. 7, 2018	A101-5	1. Add AC Coupling Capacitors of eDP AUX+/- on the carrier board.
1.20	Jun. 04, 2018	A101-5	1. Modify description of HDA_SDOUT.
1.30	Aug. 21, 2018	B101-2	1. Add SDIO function 2. Update power consumption
1.40	Sep. 10, 2018	B101-2	1. Add Differential Transitional Via Layout Recommendations.
1.50	Sep. 25, 2018	B101-2	1. Modify LPC Clock output to 24MHz.
1.60	10 25, 2019	B101-2	1. Modify PWR_BTN# description. 2. Modify power sequence request. 3. Add Input Power –Rise Time

1.6 SOM-7569 Block Diagram

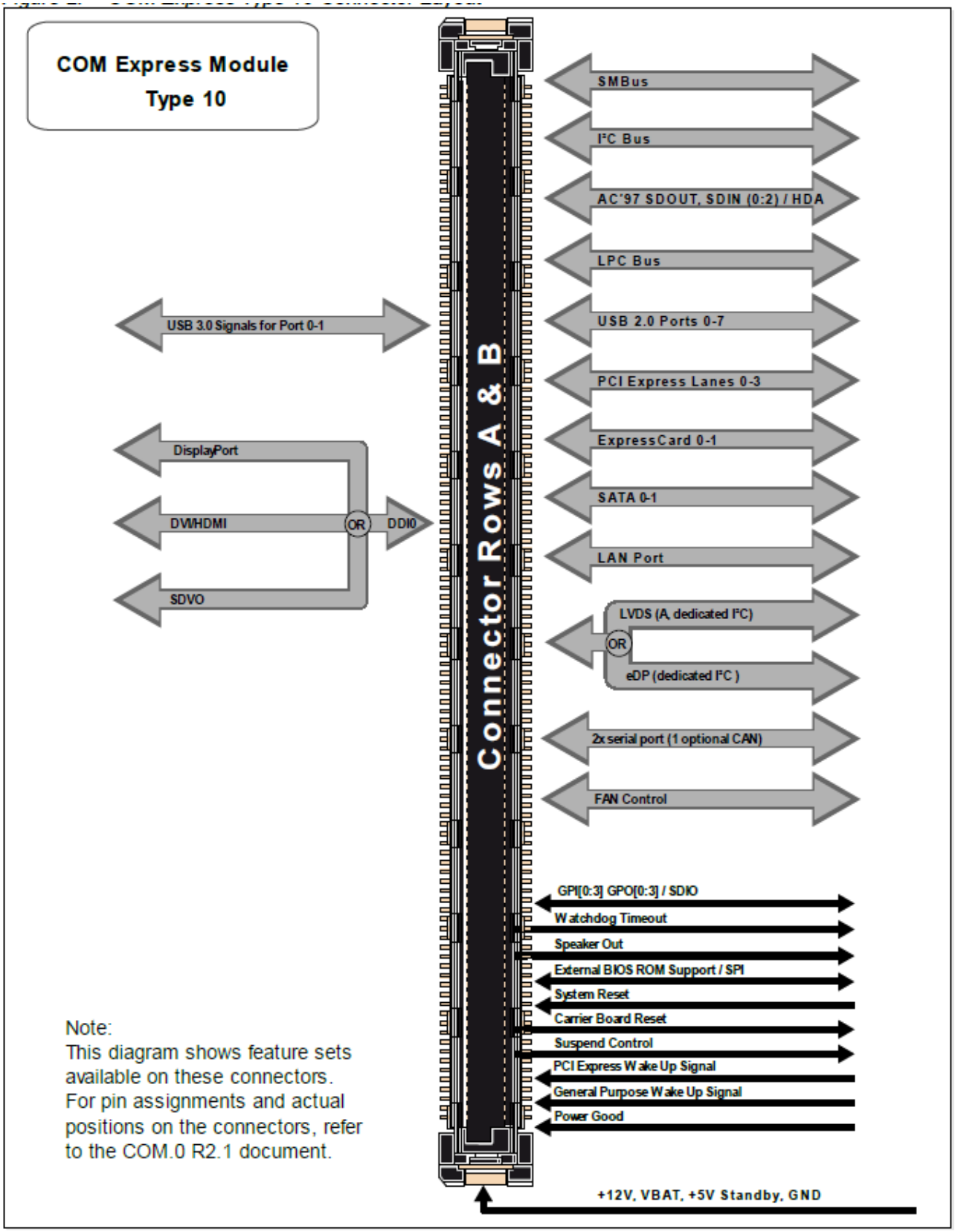
Figure 1: SOM-7569 Block Diagram



2 COM Express Type 10 Interfaces

2.1 COM Express Type 10 Connector Layout

Figure 2: COM Express Type 10 Connector Layout



2.2 COM Express Type 10 Connector Pin-out

Table 3: COM Express Type 10 Pin-out

Connector Rows A and B

Pin#	Type 10 Description	Pin#	Type 10 Description
A1	GND	B1	GND
A2	GBE0_MDI3-	B2	GBE0_ACT#
A3	GBE0_MDI3+	B3	LPC_FRAME#
A4	GBE0_LINK100#	B4	LPC_AD0
A5	GBE0_LINK1000#	B5	LPC_AD1
A6	GBE0_MDI2-	B6	LPC_AD2
A7	GBE0_MDI2+	B7	LPC_AD3
A8	GBE0_LINK#	B8	LPC_DRQ0#
A9	GBE0_MDI1-	B9	LPC_DRQ1#
A10	GBE0_MDI1+	B10	LPC_CLK
A11	GND	B11	GND
A12	GBE0_MDI0-	B12	PWRBTN#
A13	GBE0_MDI0+	B13	SMB_CK
A14	GBE0_CTREF	B14	SMB_DAT
A15	SUS_S3#	B15	SMB_ALERT#
A16	SATA0_TX+	B16	SATA1_TX+
A17	SATA0_TX	B17	SATA1_TX
A18	SUS_S4#	B18	SUS_STAT#
A19	SATA0_RX+	B19	SATA1_RX+
A20	SATA0_RX	B20	SATA1_RX-
A21	GND	B21	GND
A22	USB_SSRX0+-	B22	USB_SSTX0-
A23	USB_SSRX0+	B23	USB_SSTX0+
A24	SUS_S5#	B24	PWR_OK
A25	USB_SSRX1-	B25	USB_SSTX1-
A26	USB_SSRX1+	B26	USB_SSTX1+ -
A27	BATLOW#	B27	WDT
A28	(S)ATA_ACT#	B28	AC/HDA_SDIN2
A29	AC/HDA_SYNC	B29	AC/HDA_SDIN1
A30	AC/HDA_RST#	B30	AC/HDA_SDIN0
A31	GND	B31	GND
A32	AC/HDA_BITCLK	B32	SPKR

Connector Rows A and B

Pin#	Type 10 Description	Pin#	Type 10 Description
A33	AC/HDA_SDOUT	B33	I2C_CK
A34	BIOS_DIS0#	B34	I2C_DAT
A35	THRMTRIP#	B35	THRM#
A36	USB6-	B36	USB7-
A37	USB6+	B37	USB7+
A38	USB_6_7_OC#	B38	USB_4_5_OC#
A39	USB4-	B39	USB5-
A40	USB4+	B40	USB5+
A41	GND	B41	GND
A42	USB2-	B42	USB3-
A43	USB2+	B43	USB3+
A44	USB_2_3_OC#	B44	USB_0_1_OC#
A45	USB0-	B45	USB1-
A46	USB0+	B46	USB1+
A47	VCC_RTC	B47	EXCD1_PERST#
A48	EXCD0_PERST#	B48	EXCD1_CPPE#
A49	EXCD0_CPPE#	B49	SYS_RESET#
A50	LPC_SERIRQ	B50	CB_RESET#
A51	GND	B51	GND
A52	RSVD	B52	RSVD
A53	RSVD	B53	RSVD
A54	GPI0	B54	GPO1
A55	RSVD	B55	RSVD
A56	RSVD	B56	RSVD -
A57	GND	B57	GPO2
A58	PCIE_TX3+	B58	PCIE_RX3+
A59	PCIE_TX3-	B59	PCIE_RX3-
A60	GND	B60	GND
A61	PCIE_TX2+	B61	PCIE_RX2+
A62	PCIE_TX2-	B62	PCIE_RX2-
A63	GPI1	B63	GPO3
A64	PCIE_TX1+	B64	PCIE_RX1+
A65	PCIE_TX1-	B65	PCIE_RX1-
A66	GND	B66	WAKE0#
A67	GPI2	B67	WAKE1#

Connector Rows A and B

Pin#	Type 10 Description	Pin#	Type 10 Description
A68	PCIE_TX0+	B68	PCIE_RX0+
A69	PCIE_TX0-	B69	PCIE_RX0-
A70	GND	B70	GND
A71	LVDS_A0+	B71	DDI0_PAIR0+
A72	LVDS_A0-	B72	DDI0_PAIR0-
A73	LVDS_A1+	B73	DDI0_PAIR1+
A74	LVDS_A1-	B74	DDI0_PAIR1-
A75	LVDS_A2+	B75	DDI0_PAIR2+
A76	LVDS_A2-	B76	DDI0_PAIR2-
A77	LVDS_VDD_EN	B77	*DDI0_PAIR4+*
A78	LVDS_A3+	B78	*DDI0_PAIR4-*
A79	LVDS_A3-	B79	LVDS_BKLT_EN
A80	GND	B80	GND
A81	LVDS_A_CK+	B81	DDI0_PAIR3+
A82	LVDS_A_CK-	B82	DDI0_PAIR3-
A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL
A84	LVDS_I2C_DAT	B84	VCC_5V_SBY
A85	GPI3	B85	VCC_5V_SBY
A86	RSVD	B86	VCC_5V_SBY
A87	eDP_HPD	B87	VCC_5V_SBY
A88	PCIE_CLK_REF+	B88	BIOS_DIS1#
A89	PCIE_CLK_REF-	B89	DDI0_HPD
A90	GND	B90	GND
A91	SPI_POWER	B91	*DDI0_PAIR5+*
A92	SPI_MISO	B92	*DDI0_PAIR5-*
A93	GPO0	B93	*DDI0_PAIR6+*
A94	SPI_CLK	B94	*DDI0_PAIR6-*
A95	SPI_MOSI	B95	DDI0_DDC_AUX_SEL
A96	TPM_PP	B96	USB_HOST_PRSNT
A97	TYPE10#	B97	SPI_CS#
A98	SER0_TX	B98	DDI0_CTRLCLK_AUX+
A99	SER0_RX	B99	DDI0_CTRLDATA_AUX-
A100	GND	B100	GND
A101	SER1_TX	B101	FAN_PWMOUT
A102	SER1_RX	B102	FAN_TACHIN

Connector Rows A and B

Pin#	Type 10 Description	Pin#	Type 10 Description
A103	LID#	B103	SLEEP#
A104	VCC_12V	B104	VCC_12V
A105	VCC_12V	B105	VCC_12V
A106	VCC_12V	B106	VCC_12V
A107	VCC_12V	B107	VCC_12V
A108	VCC_12V	B108	VCC_12V
A109	VCC_12V	B109	VCC_12V
A110	GND	B110	GND

2.3 PCI Express

2.3.1 COM Express A-B Connector PCIe Groups

COM Express Type 10 Modules have only one group of PCIe lanes. This group has up to 4 PCIe Gen1/Gen2 signaling lanes.

2.3.2 General Purpose PCIe Signal Definitions

The general purpose PCI Express interface of the COM Express Type 10 Module on the COM Express A-B connector consists of up to 4 PCIe Gen1/Gen2 signaling lanes, each with a receive and transmit differential signal pair designated from PCIE_RX0 (+ and -) to PCIE_RX3 (+ and -) and correspondingly from PCIE_TX0 (+ and -) to PCIE_TX3 (+ and -). The 4 lanes may be grouped into various link widths as defined in the COM Express spec.

Table 4: General Purpose PCI Express Signal Descriptions

Signal	Pin#	Description	I/O	Note
PCIE_RX0+ PCIE_RX0-	B68 B69	PCIe channel 0. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1uF near COME to PCIE0 x1 device PETp/n0. Slot - Connect to PCIE0 x1 Conn pin A16, A17 PERp/n0. N/C if not used.	I PCIE	
PCIE_TX0+ PCIE_TX0-	A68 A69	PCIe channel 0. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE0 x1 device PERp/n0. Slot - Connect to PCIE0 x1 Conn pin B14, B15 PETp/n0. N/C if not used.	O PCIE	

Signal	Pin#	Description	I/O	Note
PCIE_RX1+ PCIE_RX1-	B64 B65	PCIe channel 1. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1uF near to PCIE1 x1 device PETp/n0. Slot - Connect to PCIE1 x1 Conn pin A16, A17 PERp/n0. N/C if not used.	I PCIE	
PCIE_TX1+ PCIE_TX1-	A64 A65	PCIe channel 1. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE1 x1 device PERp/n0. Slot - Connect to PCIE1 x1 Conn pin B14, B15 PETp/n0. N/C if not used.	O PCIE	
PCIE_RX2+ PCIE_RX2-	B61 B62	PCIe channel 2. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1uF near COME to PCIE2 x1 device PETp/n0. Slot - Connect to PCIE2 x1 Conn pin A16, A17 PERp/n0. N/C if not used.	I PCIE	
PCIE_TX2+ PCIE_TX2-	A61 A62	PCIe channel 2. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE2 x1 device PERp/n0. Slot - Connect to PCIE2 x1 Conn pin B14, B15 PETp/n0. N/C if not used.	O PCIE	
PCIE_RX3+ PCIE_RX3-	B58 B59	PCIe channel 3. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1uF near to PCIE3 x1 device PETp/n0. Slot - Connect to PCIE3 x1 Conn pin A16, A17 PERp/n0. N/C if not used.	I PCIE	

Signal	Pin#	Description	I/O	Note
PCIE_TX3+ PCIE_TX3-	A58 A59	PCIe channel 3. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE3 x1 device PERp/n0. Slot - Connect to PCIE3 x1 Conn pin B14, B15 PETp/n0. N/C if not used.	O PCIE	
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCIe Reference Clock for all COM Express PCIe lanes, and for PEG lanes. Carrier Board: Connect 0Ω in series to Device - PCIE device REFCLK+, REFCLK-. Slot - PCIE Conn pin A13 REFCLK+, A14 REFCLK-. *Connect to PCIE Clock Buffer input to provide PCIE clocks output for more than one PCIE devices or slots. N/C if not used.	O PCIE	
EXCD0_CPPE#	A49	PCI ExpressCard0: PCI Express capable card request, active low, one per card. Module has integrated PU resistor to 3.3V Express Card's CPPE# connects to Power Switch CPPE# input pin N/C if not used.	I 3.3V CMOS	
EXCD0_PERST#	A48	PCI ExpressCard0: reset, active low, one per card Express Card's PERST# and Express Card's PERST# connects to Power Switch PERST# output pin. N/C if not used.	O 3.3V CMOS	
EXCD1_CPPE#	B48	PCI ExpressCard1: PCI Express capable card request, active low, one per card. Module has integrated PU resistor to 3.3V Express Card's CPPE# connects to Power Switch CPPE# input pin N/C if not used.	I 3.3V CMOS	

Signal	Pin#	Description	I/O	Note
EXCD1_PERST#	B47	PCI ExpressCard1: reset, active low, one per card Express Card's PERST# connects to Power Switch PERST# output pin. N/C if not used	O 3.3V CMOS	
CB_RESET#	B50	Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software. Module has integrated 3.3V buffer and series resistor. Connect to reset pin of devices except PCI slots or devices. N/C if not used.	O 3.3V Suspend CMOS	
WAKE0#	B66	PCI Express wake up event signal. Module has integrated PU resistor to 3.3VDUAL Device - Connect to WAKE# pin of PCIE device. Slot - Connect to WAKE# pin B11 of PCIE slot. Express Card - Connect to WAKE# pin 11 of Express Card socket. N/C if not used.	I 3.3V Suspend CMOS	

Notes:

2.3.3 PCI Express Lane Configurations – Per COM Express Spec

According to the COM Express specification, the general purpose PCIe lanes on the A-B connector can be configured as up to 4 PCI Express x1 links or may be combined into various combinations of x4, x2 and x1 links that add up to a total of 4 lanes. These configuration possibilities are based on the COM Express Module's chip-set capabilities.

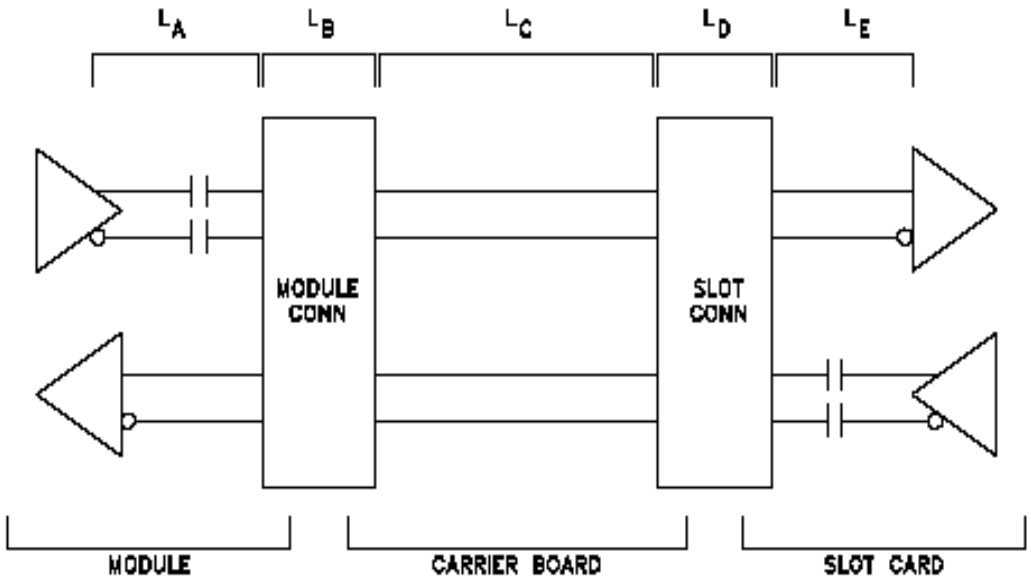
The COM Express specification defines a "fill order" from mapping PCIe links that are wider than x1 onto the COM Express pins. For example, the spec requires that a x4 PCI Express link be mapped to COM Express PCI Express lanes 0,1,2 and 3. Refer to the COM Express specification for details.

Note: All PCI Express devices are required to work in x1 mode as well as at their full capability. A x4 PCIe card for example is required by the PCI Express specification to be usable in x4 and / or x1 mode.

2.3.4 PCI Express* General Routing Guidelines

2.3.4.1 PCI Express Insertion Loss Budget with Slot Card

PCI Express Insertion Loss Budget, 1.25 GHz with Carrier Board Slot Card



The module transmit and receive insertion loss budgets are different due to the presence of the coupling caps in the module transmit path. The module transmit path insertion loss budget shall be 4.65 dB (3.46 dB + 1.19 dB). The module receive path insertion loss budget shall be 3.46 dB. COM ExpressTM connector loss is accounted for separately.

The Carrier Board transmit and receive insertion loss budgets are the same in this case. The Carrier Board insertion loss budget shall be 4.40 dB. COM ExpressTM connector and slot card connector losses are accounted for separately.

The slot card transmit and receive insertion loss budgets are different due to the presence of the coupling caps in the slot card's transmit path. The slot card's transmit path insertion loss budget is 3.84 dB (2.65 dB + 1.19 dB) per the PCI Express Card Electromechanical Specification Revision 1.1. The slot card's receive path insertion loss budget is 2.65 dB per the same specification. Slot card connector loss is accounted for separately.

Segment	**Loss (dB) max. Length [mm/inches]**	Notes
L_A	3.46 130/5.15	Allowance for 5.15 inches of module trace 3.45 dB loss @ 0.28 dB / GHz / inch and 1.66 dB crosstalk allowance. Coupling caps not included.
Coupling Caps	1.19	1.19 dB loss. From PCI Express Card Electromechanical Spec., Rev. 1.1, parameters (L_{ST} – L_{SR}). Includes crosstalk allowance of 0.79 dB.
L_B	0.25	COM Express™ connector at 1.25 GHz measured value: 0.25 dB loss.
L_C	4.4 228/9.0	Allowance for 9 inches of Carrier Board trace 4.40 db loss @ 0.28 dB / GHz / inch and a 1.25 dB crosstalk allowance.
L_D	1.25	1.25 dB loss. PCI Express Card Electromechanical Spec Rev 1.1 “guard band” allowance for slot connector – includes 1.0 dB connector loss.
L_E	2.65	2.65 dB loss. From PCI Express Card Electromechanical Spec., Rev. 1.1(without coupling caps; L_{AR}). Implied crosstalk allowance is 1.25 dB.
Total	13.20	13.20 dB loss.

PCI Express Insertion Loss Budget, 2.5 GHz with Carrier Board Slot Card

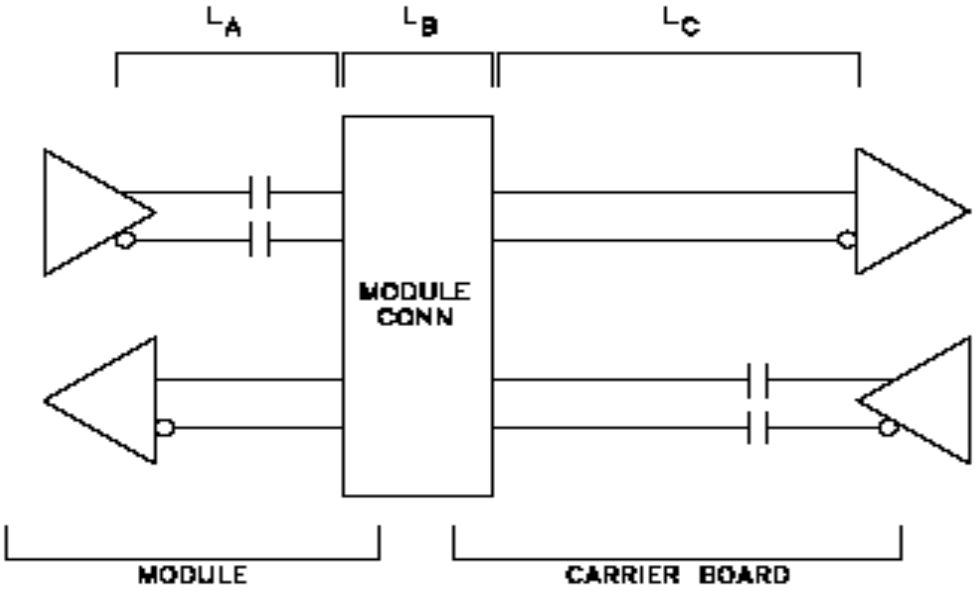
For “device up” PCIe Gen 2 operation, the Module PCIe maximum trace length is restricted to 5.0 inches and the Carrier Board maximum trace to 4.45 inches. Shorter lengths will yield additional margin and are encouraged where possible. Results assumed FR4 dielectrics.
Other dielectrics with lower losses could be considered, but were not simulated.

It should be noted that a use case exists that might result in reduced PCI Express bandwidth. This use case is tied to Carrier boards with a PCI Express slot (device up). PCI Express Gen 1 and Gen 2 signaling rates use the same PCI Express connector – there is no mechanical keying mechanism to identify the capabilities of the PCI Express slot or the PCI Express board plugged into the slot. This can lead to the situation where the Module and PCI Express board attempt a PCI Express Gen2 signaling rate connection over a Carrier that does not meet the routing guidelines for Gen 2 signaling rates. In a worst case scenario the devices might connect at Gen2 signaling rate with a high number of errors impacting the actual data throughput. It should be noted that there is a Carrier EEPROM on the Carrier which would allow the Module to determine the Carrier board capabilities but this is not a requirement in COM.0.

Segment	max. Length [mm/inches]	Notes
L_A	127/5.0	Allowance for module trace. Coupling cap effects included within simulation.
L_B		COM Express™ connector simulated at 2.5 GHz.
L_C	113/4.45	Allowance for Carrier Board.
L_D		PCI Express Card slot connector simulated at 2.5 GHz.
L_E	80/3.15	Slot Card trace length from PCI Express Card Electromagnetical Spec., Rev. 1.1
Total	320/12.6	PCIe GEN2 Data clocked architecture

2.3.4.2 PCI Express Insertion Loss Budget with Carrier Board PCIE Device

PCI Express Insertion Loss Budget, 1.25 GHz with Carrier Board PCIE Device



The module transmit and receive insertion loss budgets are different due to the presence of the coupling caps in the module transmit path. The module transmit path insertion loss budget shall be 4.65 dB (3.46 dB + 1.19 dB). The module receive path insertion loss budget shall be 3.46 dB. COM ExpressTM connector loss is accounted for separately.

The Carrier Board transmit and receive insertion loss budgets are different due to the presence of the coupling caps in the Carrier Board transmit path. The Carrier Board transmit path insertion loss budget shall be 9.49 dB (8.30 dB + 1.19 dB). The Carrier Board receive path insertion loss shall be 8.30 dB. COM ExpressTM connector loss is accounted for separately.

Segment	**Loss (dB)** **max. Length [mm/inches]**	Notes
L_A	3.46 131/5.15	Allowance for 5.15 inches of module trace 3.46 dB loss @ 0.28 dB / GHz / inch and 1.66 dB crosstalk allowance. Coupling caps not included.
Coupling Caps	1.19	1.19 dB loss. From PCI Express Card Electromechanical Spec., Rev. 1.1, parameters (LST– LSR). Includes crosstalk allowance of 0.79 dB.
L_B	0.25	COM Express™ connector at 1.25 GHz measured value: 0.25 dB loss.
L_C	8.3 113/4.45	Allowance for 15.85 inches of Carrier Board trace 8.30 dB loss @ 0.28 dB / GHz / inch and a 2.75 dB crosstalk allowance.
Total	13.2	13.2dB loss

PCI Express Insertion Loss Budget, 2.5 GHz with Carrier Board PCIE Device

For “device down” PCIe Gen 2 operation, the Module PCIe maximum trace length is restricted to 5.0 inches and the Carrier Board maximum trace to 8.0 inches. Shorter lengths will yield additional margin and are encouraged where possible. Results assumed FR4 dielectrics. Other dielectrics with lower losses could be considered, but were not simulated.

Segment	**max. Length [mm/inches]**	Notes
L_A	127/5	Allowance for module trace. Coupling cap effects included within simulation.
L_B		COM Express™ connector simulated at 2.5 GHz.
L_C	203/8	Allowance for Carrier Board trace.
Total	330/13.0	PCIe GEN2 Data clocked architecture

2.3.4.3 PCI Express Differential Transitional Via Recommendations

Transitional vias will use oval-shapes anti-pads on all plane layers. This can be created using a rectangular-shaped void to overlap with the usual round-shaped via anti-pad. The vias must also have a symmetrical trace entry.

Figure 3 and Table 5 provides the transitional differential via pad stack details.

Figure 3: Differential Transitional Via Layout

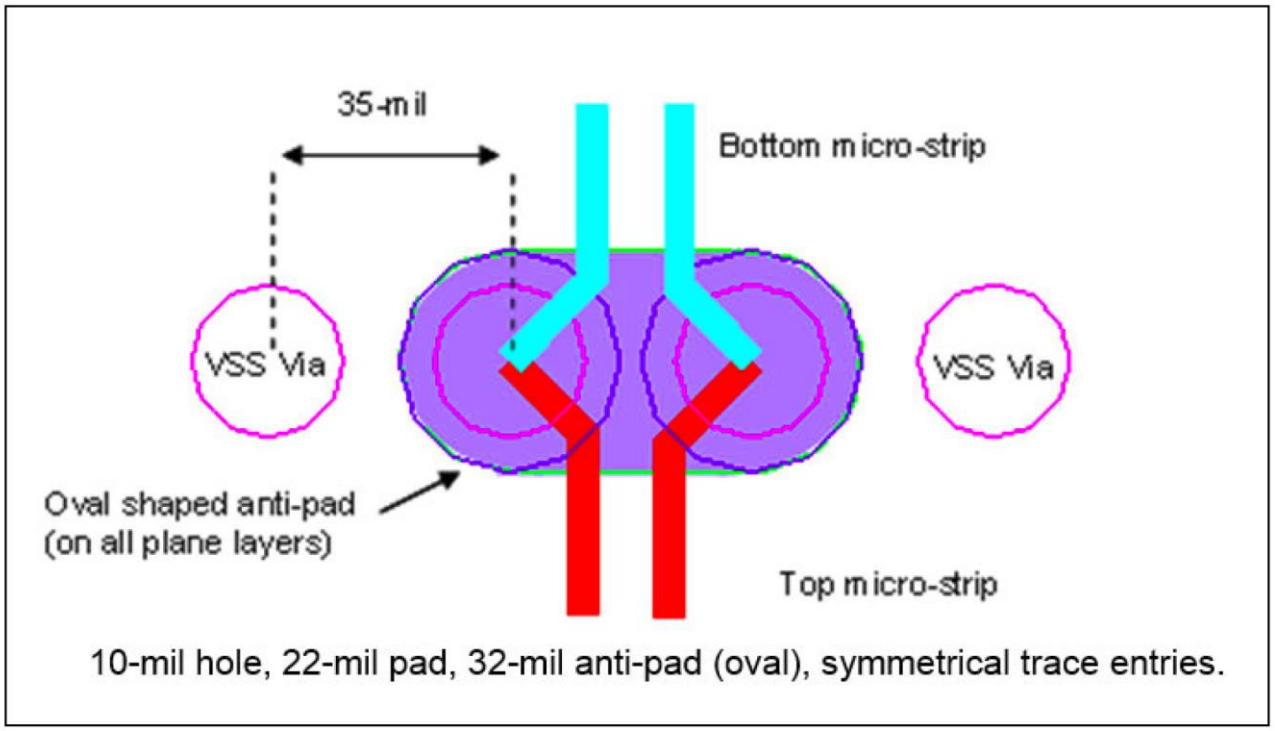


Table 5: Differential Transitional Via Layout Recommendations

Parameter	Units	Recommendation
Via Diameter	mils	10
Via Pad Size	mils	22
Oval-Shaped Anti-Pad Size	mils	32
Via to via Distance(centered)	mils	35

2.3.5 PCI Express* Trace Length Guidelines

Figure 4: Topology for PCI Express Slot Card.

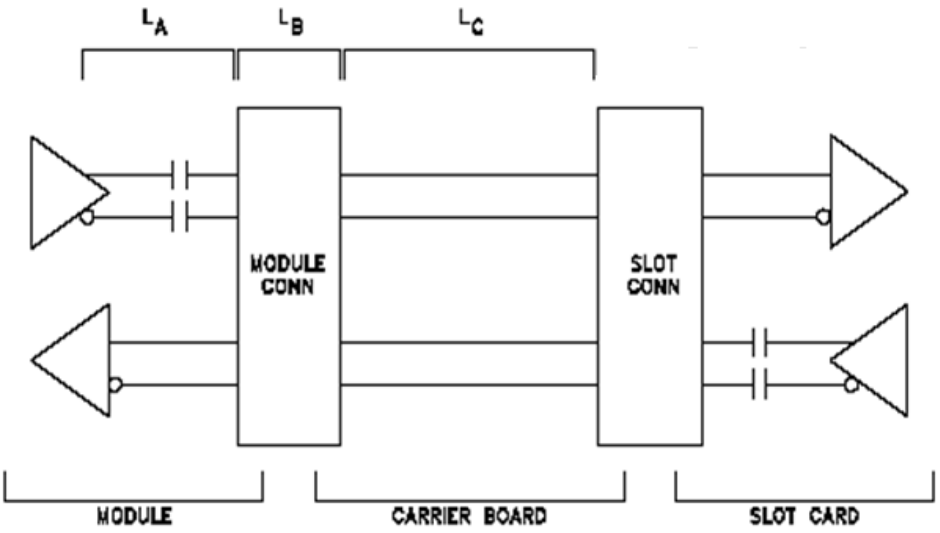


Figure 5: Topology for PCI Express Device Down.

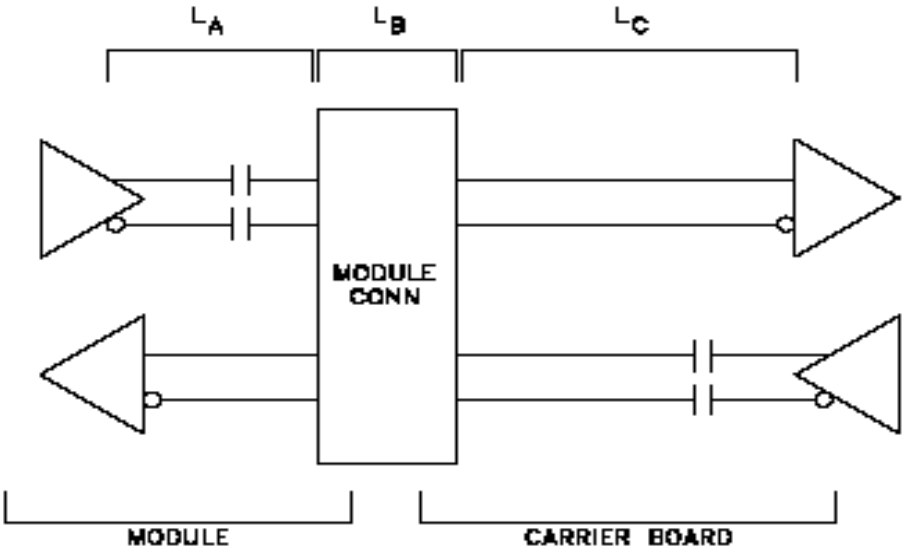


Table 6: PCI Express* Slot Card / Device Down Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	PCI Express* expansion	
Differential Impedance Target	85Ω±10%	
Single End	50Ω±10%	
Isolation to equivalent pairs	20 mils (MS) and 15 mils (DS)	
Isolation to other signal groups	20 mils (MS) and 15 mils (DS)	
Tx/Rx Spacing	20 mils	
LA + LB	Please see the SOM-7569 Layout Checklist	
Lc	Carrier Board Length	
Max length of LA+LB+LC	Slot Card: 8” (Gen2) Device Down: 10” (Gen2)	
Length matching	Differential pairs (intra-pair): Max. ±5 mils REFCLK+ and REFCLK- (intra-pair):Max. ±20mils	
Reference Plane	GND referencing preferred Min 40-mil trace edge-to-major plane edge spacing GND stitching vias required next to signal vias if transitioning layers between GND layers Power referencing acceptable if stitching caps are used	
Carrier Board Via Usage	Max. 2 vias per TX trace, Max. 4 vias per RX trace	
AC coupling	The AC coupling capacitors for the TX lines are incorporated on the COM Express Module. The AC coupling capacitors for RX signal lines have to be implemented on the customer COM Express Carrier Board. Capacitor type: X7R, 100nF ±10%, 16V, shape 0402.	1

Notes:

1. AC caps are recommended to be placed close to PCIe device side (avoid placing AC cpas on mid-bus).

2.4 Digital Display Interfaces (DDI)

Module Types 10 use Digital Display Interfaces (DDI) to provide DisplayPort, HDMI/DVI, and SDVO interfaces. Type 10 Modules can contain a single DDI (DDI[0]) that can support DisplayPort, HDMI/DVI, and SDVO.

The main difference is that SDVO is only supported DDI[0] for Type 10 Modules.

DisplayPort / HDMI / DVI

DisplayPort was developed by the Video Electronics Standard Association (VESA) in order to create a new digital display port interface to connect a video source to a display device.

DisplayPort can be used to transfer audio and video at the same time, but each one is optional and can be transmitted without the other. A bi-directional, half-duplex auxiliary channel carries device anagement and device control data for the Main Link, such as VESA EDID.

DisplayPort is nowadays on almost all COM Express Modules available as Dual-mode DisplayPort, that can directly emit single-link HDMI and DVI signals using an adapter, which contains a level shifter to adjust for the lower voltages required by DisplayPort. These adapters can be directly implemented on the Carrier Board to have an easy, simple and future proof implementation of HDMI and/or DVI or an inexpensive cable adapter can be directly connectedon the Carrier Board's DisplayPort connector.

2.4.1 DDI Signal Definitions

Type 10 offers up to one DisplayPort interfaces.

Each DisplayPort interface consists of 4 differential lanes, 1 auxiliary lane and 1 hot-plug-detect signal. The DDC_AUX_SEL pin should be routed to pin 13 of the DisplayPort connector, to enable Dual-Mode. When HDMI/DVI is directly done on the Carrier Board, this pin shall be pulled to 3.3V with a 100k Ohm resistor to configure the AUX pairs as DDC channels.

Table 7: Port / HDMI / DVI Pin-out of Type 10

Pin Name	DDI0 Pin#	Function (DDIX) DisplayPort	Function (DDIX) HDMI / DVI
DDIX_PAIR0+	B71	DPX_LANE0+	TMDSX_DATA2+
DDIX_PAIR0-	B72	DPX_LANE0-	TMDSX_DATA2-
DDIX_PAIR1+	B73	DPX_LANE1+	TMDSX_DATA1+
DDIX_PAIR1-	B74	DPX_LANE1-	TMDSX_DATA1-
DDIX_PAIR2+	B75	DPX_LANE2+	TMDSX_DATA0+
DDIX_PAIR2-	B76	DPX_LANE2-	TMDSX_DATA0-
DDIX_PAIR3+	B81	DPX_LANE3+	TMDSX_CLK+
DDIX_PAIR3-	B82	DPX_LANE3-	TMDSX_CLK-
DDIX_HPD	B89	DPX_HPD	HDMIX_HPD
DDIX_CTRLCLK_AUX+	B98	DPX_AUX+	HDMIX_CTRLCLK
DDIX_CTRLCLK_AUX-	B99	DPX_AUX-	HDMIX_CTRLDATA
DDIX_DDC_AUX_SEL	B95		

Note: Please verify in the Module's specification if DisplayPort or Dual-Mode DisplayPort is supported.

Table 8: DDI0 Signal Description

Signal	Pin#	Description	I/O	Notes
DDI0_PAIR0+ DDI0_PAIR0-	B71 B72	DDI channel 0, differential pairs 0. Carrier Board: For DP, connect AC Coupling Capacitors 75~200 nF near COME to device or DP connector. For HDMI / DVI, connect AC Coupling Capacitors 75~200 nF near COME and Level Shifter to HDMI or DVI connector. N/C if not used.	O PCIE	
DDI0_PAIR1+ DDI0_PAIR1-	B73 B74	DDI channel 0, differential pairs 1. Carrier Board: For DP, connect AC Coupling Capacitors 75~200 nF near COME to device or DP connector. For HDMI / DVI, connect AC Coupling Capacitors 75~200 nF near COME and Level Shifter to HDMI or DVI connector. N/C if not used.	O PCIE	
DDI0_PAIR2+ DDI0_PAIR2-	B75 B76	DDI channel 0, differential pairs 2. Carrier Board: For DP, connect AC Coupling Capacitors 75~200 nF near COME to device or DP connector. For HDMI / DVI, connect AC Coupling Capacitors 75~200 nF near COME and Level Shifter to HDMI or DVI connector. N/C if not used.	O PCIE	
DDI0_PAIR3+ DDI0_PAIR3-	B81 B82	DDI channel 0, differential pairs 3. Carrier Board: For DP, connect AC Coupling Capacitors 75~200 nF near COME to device or DP connector. For HDMI / DVI, connect AC Coupling Capacitors 75~200 nF near COME and Level Shifter to HDMI or DVI connector. N/C if not used.	O PCIE	

Signal	Pin#	Description	I/O	Notes
DDI0_HPD	B89	DDI channel 0, Hot-Plug Detect. Module has integrated current blocking circuit and PD resistor to GND Carrier Board: For DP, connector to device or DP connector HP pin. For HDMI / DVI, connect 3.3V to 5V Level Shifter to device, HDMI or DVI PD ping. NC if not used.	I 3.3V COMS	
DDI0_CTRLCLK_AUX+ DDI0_CTRLCLK_AUX-	B98 B99	DDI channel0, DP AUX function. DDC_AUX_SEL is no connect. Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access. Module has integrated AC Coupling Capacitor , AUX+ PD resistor to GND and AUX- PU to 3.3V Carrier Board: Connect to device or DP connector. N/C if not used.	I/O PCIE	
		DDI channel0, HDMI / DVI I²C function. DDC_AUX_SEL is pulled high. Carrier Board: Connect 3.3V-5V Level Shifter to device, HDMI or DVI connector. N/C if not used.	I/O OD 3.3V COMS	
DDI0_DDC_AUX_SEL	B95	Selects the function of DDI0_CTRLCLK_AUX+ and DDI0_CTRLDATA_AUX-. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals. Module has integrated PD resistor to GND. Carrier Board: DP1 AUX+/- - N/C HDMI1: PU 100K to 3.3V N/C if not used.	I 3.3V COMS	

Notes:

2.4.2 Digital Display Interfaces (DDI) Routing Guidelines

2.4.2.1 DisplayPort Routing Guidelines

Carriers that support DisplayPort (DisplayPort only or dual mode):

- DC blocking capacitors shall be placed on the Carrier for the DDI[n]_PAIR[0:3] signals.
- The Carrier shall include a blocking FET on DDI[n]_HPD to prevent back-drive current from damaging the Module.

When implementing DisplayPort on the Carrier Board, the DP_AUX+ line shall have a pulldown resistor to GND. The resistor value should be 100kΩ. The DP_AUX- line shall have a pull-up resistor to 2.5V. The resistor value should be 100kΩ. The resistors shall be placed on the DisplayPort connector side of the AC coupling capacitors. The DP_HP signal shall include a blocking FET to prevent back-drive current damage. The DP_HP signal shall be pulled-down to GND with a 110kΩ resistor.

The DDI signals can be used to support a variety of video interfaces. The circuits required to realize the different video interfaces will be determined by a future PICMG Carrier Design Guide subcommittee. At this time, they only requirement placed on Modules for the DDI signals is the maximum trace length specified below.

Figure 6: DisplayPort Loss Budget

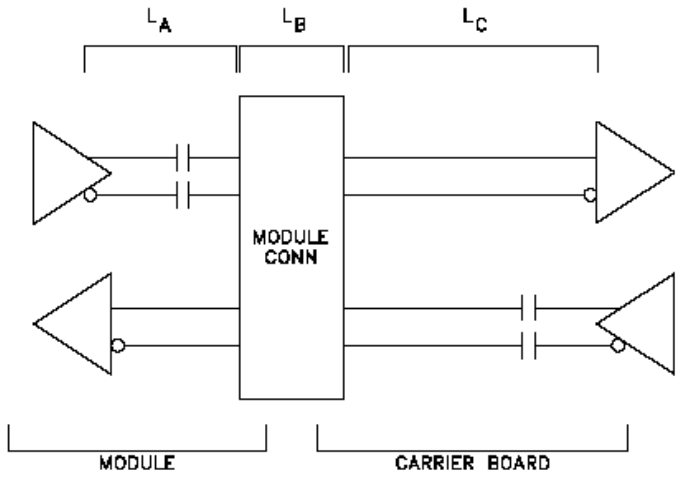


Table 9: DisplayPort Insertion Loss Budget

Segment	max. Length [mm/inches]	Notes
L_A	127/5.0	Allowance for module trace. Coupling cap effects included within simulation.
L_B		COM Express™ connector simulated at 2.5 GHz.
L_C	TBD	Allowance for Carrier Board trace.
Total	TBD	

Figure 7: Topology for DisplayPort

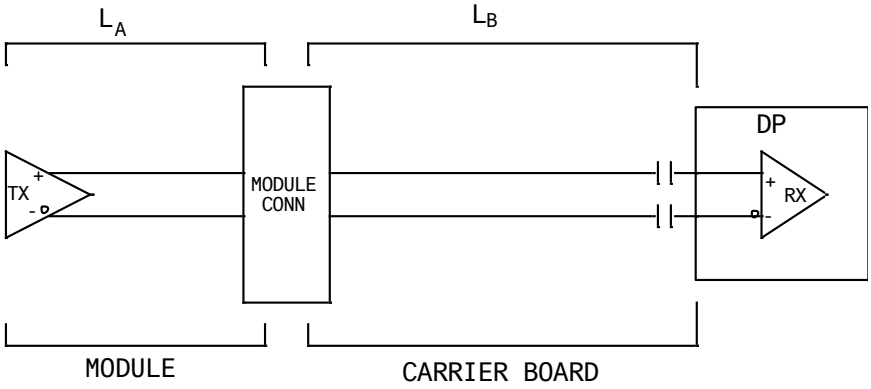


Table 10: DisplayPort Connector / Device Down Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	DisplayPort	
Differential Impedance Target	85 Ω ±10%	
Single End	50Ω ±10%	
Isolation to equivalent pairs	20 mils (MS) and 15 mils (DS)	
Isolation to other signal groups	20 mils (MS) and 15 mils (DS)	
LA	Please see the SOM-7569 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	DDI differential pairs to DP connector: 6.5” AUX channel: 10”	
Length matching	Differential pairs (intra-pair): Max. ±5 mils For each channel, match the lengths of the differential pairs (Inter-Pair) to be within a 1-inch	2
Reference Plane	GND referencing preferred. Min 40-mil trace edge-to-major plane edge spacing.	
Carrier Board Via Usage	Max. 2 vias.	
AC coupling	Min = 75 nF Max = 200 nF	1

Notes:

1. AC caps are recommended to be placed close to device side (avoid placing AC cpas on mid-bus).
2. AUX channel length matching between DDI differential pairs: Max. 500 mils

2.4.2.2 HDMI / DVI Routing Guidelines

When implementing HDMI level shifters shall be used on the TMDS signals. Bi-directional level shifters shall be used between the 3.3V and 5V CTRLCLK and CTRLDATA signals with 2.2kΩ pull-ups to 3.3V and 5V.

Carriers that support TMDS (DVI/HDMI):

- DDI[n]_DDC_AUX_SEL shall be pulled to 3.3V on the Carrier with a 100K Ohm resistor to configure the DDI[n]_AUX pair as the DDC channel.
- Bi-directional level translators shall be placed on the Carrier DDI[n]_CTRLDATA_AUX- and DDI[n]_CTRLCLK_AUX+ to convert the 3.3V DDC channel on the Module to the 5V DDC channel for the TMDS display.
- Pull-up resistors shall be placed on the Carrier from 3.3V (Module side of level translator) and 5V (display side of level translator) and the [n]_CTRLDATA_AUX- and DI[n]_CTRLCLK_AUX+ signals. The pull-up resistor should be 2k.
- Level translators Shall be placed on the Carrier DDI[n]_PAIR[0:3] signals.
- DC blocking capacitors shall be placed on the Carrier for the DDI[n]_PAIR[0:3] signals.
- The Carrier shall include a blocking FET on DDI[n]_HPD to prevent back-drive current from damaging the module.

The DDI signals can be used to support a variety of video interfaces. The circuits required to realize the different video interfaces will be determined by a future PICMG Carrier Design Guide subcommittee. At this time, they only requirement placed on Modules for the DDI signals is the maximum trace length specified below.

Figure 8: HDMI / DVI (TMDS) Loss Budget

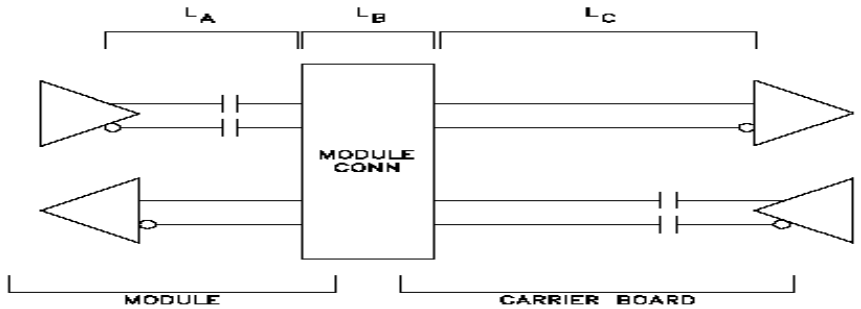


Table 11: HDMI / DVI (TMDS) Insertion Loss Budget

Segment	max. Length [mm/inches]	Notes
L_A	127/5.0	Allowance for module trace. Coupling cap effects included within simulation.
L_B		COM Express™ connector simulated at 2.5 GHz.
L_C	TBD	Allowance for Carrier Board trace.
Total	TBD	

Figure 9: Topology for HDMI / DVI

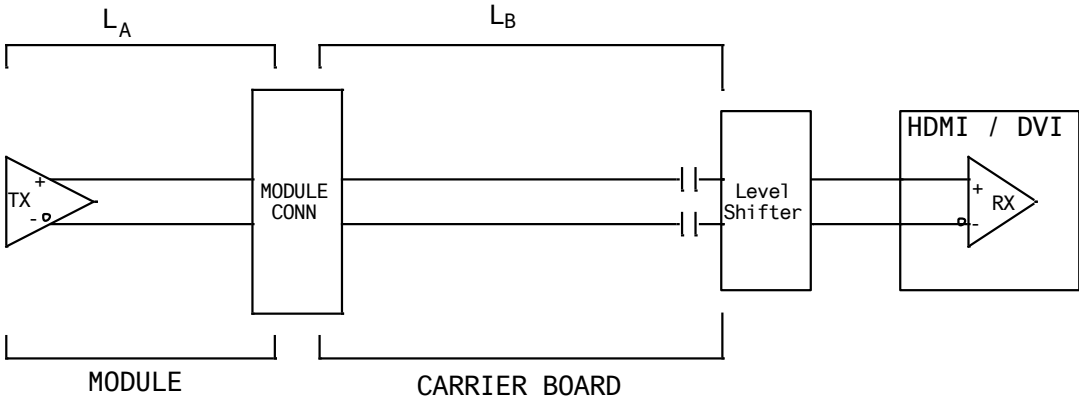


Table 12: HDMI / DVI Connector / Device Down Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	HDMI / DVI (TMDS)	
Differential Impedance Target	85 Ω ±10%	
Single End	50Ω ±10%	
Isolation to equivalent pairs	20 mils (MS) and 15 mils (DS)	
Isolation to other signal groups	20 mils (MS) and 15 mils (DS)	
LA	Please see the SOM-7569 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	DDI differential pairs to Active Level Shifter: 7.” DDI differential pairs to Cost Reduce Level Shifter: 4.6” DDC channel: 10”	
Length matching	Differential pairs (intra-pair): Max. ±5 mils For each channel, Maximum length mismatch between data lanes is 1000 mils. CTRDATA - CTRCLK < 1000 mil	
Reference Plane	GND referencing preferred. Min 40-mil trace edge-to-major plane edge spacing.	
Carrier Board Via Usage	Max. 2 vias.	
AC coupling	Min = 75 nF Max = 200 nF	1

Notes:

1. AC caps are recommended to be placed close to device side (avoid placing AC cpas on mid-bus).

2.4.3 HDMI / DVI Level Shifter Requirements

The HDMI specification requires the receiver to be terminated to AVCC (nominally 3.3 V) through Rt (nominally 50 Ω). The HDMI receiver requirements require the native HDMI signals from the SOC to be level shifted. This prevents electrical overstress of the driver and ensure that the receiver is operational within the receiver specifications defined in the *High Definition Multimedia Interface Specification 1.4a*.

2.4.4 ESD Protection

HDMI signals are subjected to ESD strikes due to plugging in of the devices through the HDMI cable and frequent human contact that can destroy both the HDMI host and devices on the platform. Therefore these ports need to be protected.

There are a wide variety of ESD protection devices and ESD suppressors readily available in the market such as Metal Oxide Varistors (MOVs), Zener Diode, Transient Voltage Suppressor (TVS), Polymer devices and ESD diode arrays. With 1.65 Gbps of data rate, HDMI is very sensitive to parasitic capacitance. Excessive parasitic capacitance can severely degrade the signal integrity and lead to a compliance or operational failure. To maintain signal integrity, Intel recommends to use ESD suppressors or diode arrays having a low junction capacitance.

Recommended characteristics of an ideal ESD Protection Diode for HDMI:

- Able to withstand at least 8 kV of ESD strikes.
- Low capacitance <1 pF to minimize signal distortion at high data rates as higher capacitance degrade the HDMI signal quality.
- Fast response/rise time to protect from the fast rise time of ESD surge pulses.
- Low-leakage current to minimize static power consumption.
- Ensure the selected ESD solution will not violate HDMI Voff spec. In a low power state a power rail ESD diode can become forward biased as a result on the HDMI sink (panel) termination of 50 Ω to 3.3 V
- Some ESD devices may impact the trace impedance. Care should be taken while choosing such devices so that the differential-impedance target in the *HDMI 1.4 Specification* is not violated.

The *HDMI 1.4a Specification* requires that 8 kV of ESD strikes be tolerated.

The ESD protection devices should be placed as close to the HDMI connector as possible so that when ESD strikes occur, the discharges can be quickly absorbed or diverted to the ground/power plane before it is coupled to another signal path nearby.
Footprints for ESD components or diode arrays can be provided on board with no stubs and no more than 750 mils (19.05 mm) from the connector. The ESD components can be stuffed depending on the requirement.

2.5 LAN Interface

All COM Express Modules provide at least one LAN port. The 8-wire 10/100/1000BASE-T Gigabit Ethernet interface compliant to the IEEE 802.3-2005 specification is the preferred interface for this port, with the COM Express Module PHY responsible for implementing auto-negotiation of 10/100BASE-TX vs 10/100/1000BASE-T operation. The carrier may also support a 4-wire 10/100BASE-TX interface from the COM Express Module on an exception basis. Check with your vendor for 10/100 only implementations.

2.5.1 LAN Signal Definitions

The LAN interface of the COM Express Module consists of 4 pairs of low voltage differential pair signals designated from *'GBE0_MDI0'* (+ and -) to *'GBE0_MDI3'* (+ and -) plus additional control signals for link activity indicators. These signals can be used to connect to a 10/100/1000BASE-T RJ45 connector with integrated or external isolation magnetics on the Carrier Board. The corresponding LAN differential pair and control signals can be found on rows A and B of the Module's connector.

Table 13: LAN Interface Signal Descriptions

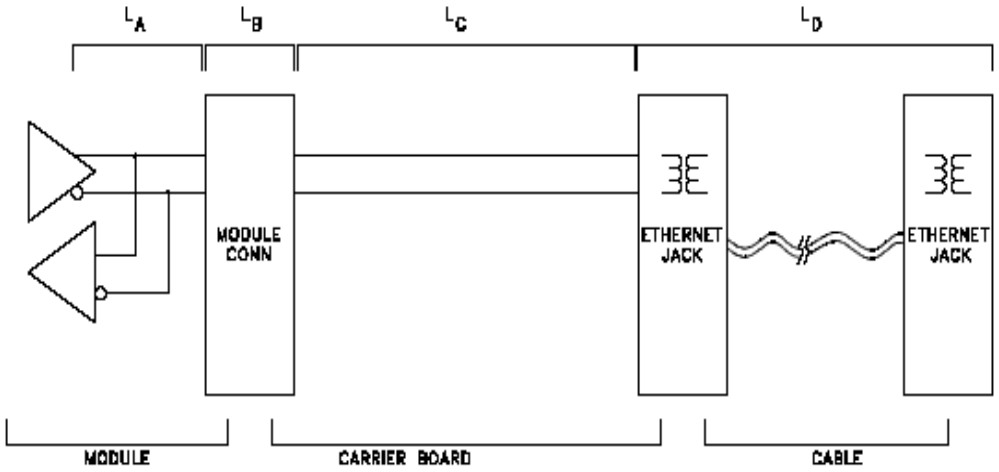
Signal	Pin#	Description	I/O	Note
GBE0_MDI0+ GBE0_MDI0-	A13 A12	Media Dependent Interface (MDI) differential pair 0. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Module has integrated termination. Carrier Board: Connect to Magnetics Module MDI0+/- N/C if not used.	I/O GBE	
GBE0_MDI1+ GBE0_MDI1-	A10 A9	Media Dependent Interface (MDI) differential pair 1. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Module has integrated termination. Carrier Board: Connect to Magnetics Module MDI0+/- N/C if not used	I/O GBE	

Signal	Pin#	Description	I/O	Note
GBE0_MDI2+ GBE0_MDI02	A7 A6	Media Dependent Interface (MDI) differential pair 2. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Module has integrated termination. Carrier Board: Connect to Magnetics Module MDI2+/- N/C if not used.	I/O GBE	
GBE0_MDI3+ GBE0_MDI3-	A3 A2	Media Dependent Interface (MDI) differential pair 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Module has integrated termination. Carrier Board: Connect to Magnetics Module MDI3+/- N/C if not used	I/O GBE	
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. Carrier Board: 0.1uF to ground. N/C if not used.	REF	
GBE0_LINK#	A8	Ethernet controller 0 link indicator, active low.	O 3.3V Suspend / 3.3V OD CMOS	
GBE0_LINK100#	A4	Ethernet controller 0 100Mbit/sec link indicator, active low.	O 3.3V Suspend / 3.3V OD CMOS	
GBE0_LINK1000#	A5	Ethernet controller 0 1000Mbit/sec link indicator, active low.	O 3.3V Suspend / 3.3V OD CMO	
GBE0_ACT#	B2	Ethernet controller 0 activity indicator, active low.	O 3.3V Suspend / 3.3V OD CMO	

2.5.2 LAN Routing Guidelines

10/100/1000 Ethernet Insertion Loss Budget

Figure 10: 10/100/1000 Ethernet Insertion Loss Budget



COM ExpressTM Ethernet implementations should conform to insertion loss values less than or equal to those shown in the table above. The insertion loss values shown account for frequency dependent material losses only. Cross talk losses are separate from material losses in the Gb Ethernet pecification.

“Device Down” implementations, in which the Ethernet target device is implemented on the Carrier Board (for instance, an Ethernet switch), may add the insertion loss for the RJ45 Ethernet jack and integrated magnetics to the Carrier Board budget. This insertion loss value is typically 1 dB. The Carrier Board insertion loss budget then becomes LC + 1 dB, or 1.15 dB.

Table 14: 10/100/1000 Ethernet Insertion Loss Budget, 100 MHz

Segment	Loss (dB)	Notes
L_A	0.08	Up to 3 inches of module trace @ 0.28 dB / GHz / inch
L_B	0.02	COM Express™ connector at 100 MHz measured value
L_C	0.15	Up to 5 inches of Carrier Board trace @ 0.28 dB / GHz / inch
L_D	24.00	Cable and cable connectors, integrated magnetics, per source spec.
Total	24.25	

2.5.3 LAN Trace Length Guidelines

Figure 11: Topology for Ethernet Jack

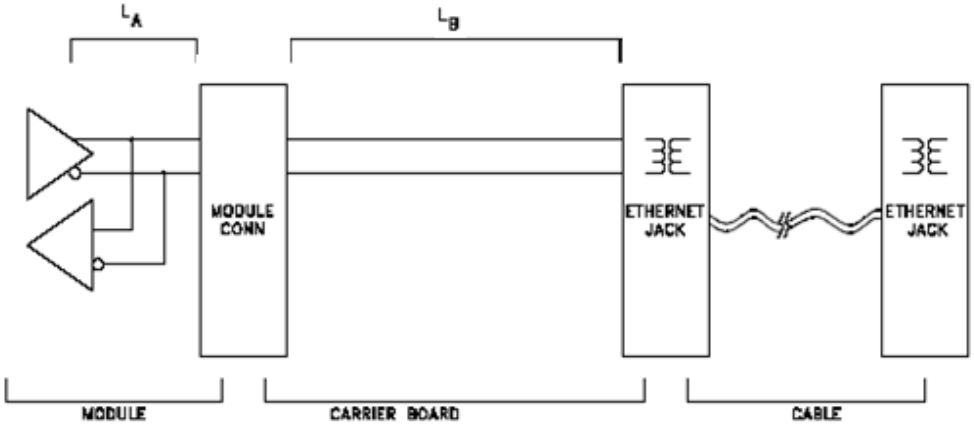


Table 15: Ethernet Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	GBE0_MDIx+, GBE0_MDIx-	
Differential Impedance Target	100 Ω ±10%	
Single End	50Ω ±10%	
Spacing between RX and TX pairs (inter-pair) (s)	Min. 50mils	
Spacing between differential pairs and high-speed periodic signals	Min. 300mils	
Spacing between differential pairs and low-speed non periodic signals	Min. 100mils	
Spacing between digital ground and analog ground plane (between the magnetics Module and RJ45 connector)	Min. 60mils	
LA	Please see the SOM-7569 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	COM Express Module to the magnetics Module - 5.0 inches. Magnetics Module to RJ45 connector - Max. 1.0 inches.	
Length matching	Differential pairs (intra-pair): Max. ±10 mils RX and TX pairs (inter-pair) - Max. ±2000 mils	
Reference Plane	GND referencing preferred.	
Spacing from edge of plane	Min. 40mils	
Carrier Board Via Usage	Max. 2 vias.	

Notes:

2.5.4 Reference Ground Isolation and Coupling

The Carrier Board should maintain a well-designed analog ground plane around the components on the primary side of the transformer between the transformer and the RJ-45 receptacle. The analog ground plane is bonded to the shield of the external cable through the RJ-45 connector housing.

The analog ground plane should be coupled to the carrier's digital logic ground plane using a capacitive coupling circuit that meets the ground plane isolation requirements defined in the 802.3-2005 specification. It is recommended that the Carrier Board PCB design maintain a minimum 30 mil gap between the digital logic ground plane and the analog ground plane.

It's recommended to place an optional GND to SHIELDGND connection near the RJ-45 connector to improve EMI and ESD capabilities.

2.6 USB2.0 Ports

A COM Express Module must support a minimum of 4 USB Ports and can support up to 8 USB Ports. All of the USB Ports must be USB2.0 compliant. There are 4 over-current signals shared by the 8 USB Ports. A Carrier must current limit the USB power source to minimize disruption of the Carrier in the event that a short or over-current condition exists on one of the USB Ports. A Module must fill the USB Ports starting at Port 0. The USB SuperSpeed ports 0 and 1, if used, are to be paired with USB 2.0 ports 0 and 1in the same order. The USB SuperSpeed ports use the same over current signaling mechanism as the USB 2.0 ports, but USB 3.0 allows up to 1A current per port instead of 500mA allowed in USB 2.0. Although USB 2.0 signals use differential signaling, the USB specification also encodes single ended state information in the differential pair, making EMI filtering somewhat challenging. Ports that are internal to the Carrier do not need EMI filters. A USB Port can be powered from the Carrier Main Power or from the Carrier Suspend Power. Main Power is used for USB devices that are accessed when the system is powered on. Suspend Power (VCC_5V_SBY) is used for devices that need to be powered when the Module is in Sleep-State S5. This would typically be for USB devices that support Wake-on-USB. The amount of current available on VCC_5V_SBY is limited so it should be used sparingly.

2.6.1 USB2.0 Signal Definitions

Table 16: USB Signal Descriptions

Signal	Pin#	Description	I/O	Note
USB0+ USB0-	A46 A45	USB Port 0, data + or D+ USB Port 0, data + or D- Carrier board: Device - Connect to D+/- Conn. - Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to Pin 3 D+ / Pin 2 D- N/C if not used	I/O USB	
USB1+ USB1-	B46 B45	USB Port 1, data + or D+ USB Port 1, data + or D- Carrier board: Device - Connect to D+/- Conn. - Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to Pin 3 D+ / Pin 2 D- N/C if not used	I/O USB	

Signal	Pin#	Description	I/O	Note
USB2+ USB2-	A43 A42	USB Port 2, data + or D+ USB Port 2, data + or D- Carrier board: Device - Connect to D+/- Conn. - Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to Pin 3 D+ / Pin 2 D- N/C if not used	I/O USB	
USB3+ USB3-	B43 B42	USB Port 3, data + or D+ USB Port 3, data + or D- Carrier board: Device - Connect to D+/- Conn. - Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to Pin 3 D+ / Pin 2 D- N/C if not used	I/O USB	
USB4+ USB4-	A40 A39	USB Port 4, data + or D+ USB Port 4, data + or D- Carrier board: Device - Connect to D+/- Conn. - Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to Pin 3 D+ / Pin 2 D- N/C if not used	I/O USB	
USB5+ USB5-	B40 B39	USB Port 5, data + or D+ USB Port 5, data + or D- Carrier board: Device - Connect to D+/- Conn. - Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to Pin 3 D+ / Pin 2 D- N/C if not used	I/O USB	
USB6+ USB6-	A37 A36	USB Port 6, data + or D+ USB Port 6, data + or D- Carrier board: Device - Connect to D+/- Conn. - Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to Pin 3 D+ / Pin 2 D- N/C if not used	I/O USB	

Signal	Pin#	Description	I/O	Note
USB7+ USB7-	B37 B36	USB Port 7, data + or D+ USB Port 7, data + or D- Carrier Board: Device - Connect to D+/- Conn. - Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to Pin 3 D+ / Pin 2 D- N/C if not used	I/O USB	
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1. Carrier Board: Connect to Overcurrent of Power Distribution Switch and Bypass 0.1uF to GND N/C if not used	I 3.3V CMOS	1
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3. Carrier Board: Connect to Overcurrent of Power Distribution Switch and Bypass 0.1uF to GND N/C if not used	I 3.3V CMOS	1
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5. Carrier Board: Connect to Overcurrent of Power Distribution Switch and Bypass 0.1uF to GND N/C if not used	I 3.3V CMOS	2
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7. Carrier Board: Connect to Overcurrent of Power Distribution Switch and Bypass 0.1uF to GND N/C if not used	I 3.3V CMOS	2
USB_HOST_PRSINT	B96	Module USB client may detect the presence of a USB host. A high value indicates that a host is present. Carrier Board: USB Conn. Pin 1 connects to 1. Clampling diode, 1uF and 100KΩ to GND. 2. 5V to 3.3V level shifter circuit to COME USB_HOST_PRSNT. N/C if not used	I 3.3V CMOS	

Notes:

1. SOM-7569 was tied USB_0_1_OC# & USB_2_3_OC# together.
2. SOM-7569 was tied USB_4_5_OC# & USB_6_7_OC# together.

2.6.1.1 USB Over-Current Protection (USB_x_y_OC#)

The USB Specification describes power distribution over the USB port, which supplies power for USB devices that are directly connected to the Carrier Board. Therefore, the host must implement over-current protection on the ports for safety reasons. Should the aggregate current drawn by the downstream ports exceed a permitted value, the over-current protection circuit removes power from all affected downstream ports. The over-current limiting mechanism must be resettable without user mechanical intervention. For more detailed information about this subject, refer to the 'Universal Serial Bus Specifications Revision 2.0', which can be found on the website http://www.usb.org.

Over-current protection for USB ports can be implemented by using power distribution switches on the Carrier Board that monitor the USB port power lines. Power distribution switches usually have a soft-start circuitry that minimizes inrush current in applications where highly capacitive loads are employed. Transient faults are internally filtered.

Additionally, they offer a fault status output that is asserted during over-current and thermal shutdown conditions. These outputs should be connected to the corresponding COM Express Modules USB over-current sense signals. Fault status signaling is an option at the USB specification. If you don't need the popup message in your OS you may leave the signals USB_0_1_OC#, USB_2_3_OC#, USB_4_5_OC# and USB_6_7_OC# unconnected.

Simple resettable PolySwitch devices are capable of fulfilling the requirements of USB overcurrent protection and therefore can be used as a replacement for power distribution switches.
Fault status signals are connected by a pullup resistor to VCC_3V3_SBY on COM Express Module. Please check your tolerance on a USB port with VCC_5V supply.

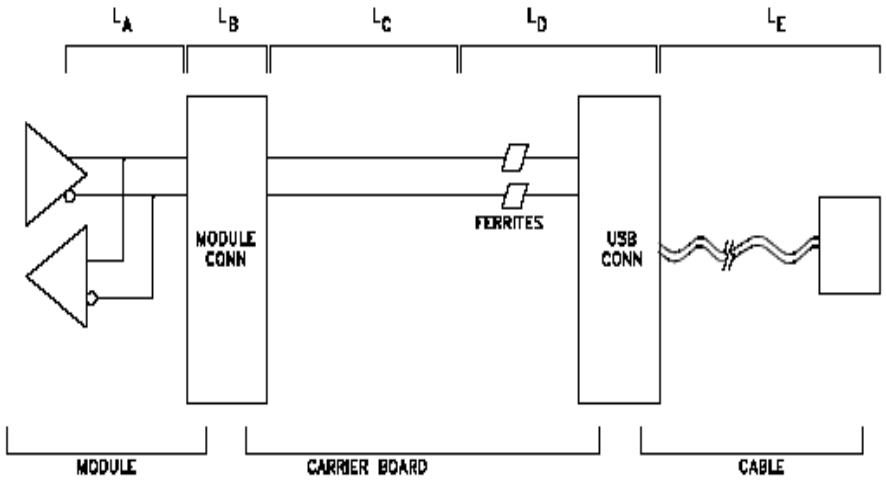
2.6.1.2 Powering USB devices during S5

The power distribution switches and the ESD protection shown in the schematics can be powered from Main Power or Suspend Power (VCC_5V_SBY). Ports powered by Suspend Power are powered during the S3 and S5 system states. This provides the ability for the COM Express Module to generate system wake-up events over the USB interface.

2.6.2 USB2.0 Routing Guidelines

USB Insertion Loss Budget

Figure 12: USB Insertion Loss Budget



COM ExpressTM USB implementations should conform to insertion loss values less than or equal to those shown in the table above. The insertion loss values shown account for frequency dependent material losses only. Cross talk losses are separate from material losses in the USB specification.

"Device Down" implementations, in which the USB target device is implemented on the Carrier Board, may add the ferrite and USB connector insertion loss values to the Carrier Board budget.

The Carrier Board insertion loss budget then becomes LC + LD, or 2.68 dB.

Table 17 : USB Insertion Loss Budget, 400 MHz

Segment	Loss (dB)	Notes
L_A	0.67	Up to 6 inches of module trace @ 0.28 dB / GHz / inch
L_B	0.05	COM ExpressTM connector at 400 MHz measured value
L_C	1.68	Up to 14 inches of Carrier Board trace @ 0.28 dB / GHz / inch
L_D	1.00	USB connector and ferrite loss
L_E	5.80	USB cable and far end connector loss, per source specification
Total	9.20	

2.6.2.1 USB 2.0 General Design Considerations and Optimization

Use the following general routing and placement guidelines when laying out a new design. These guidelines help minimize signal quality and EMI problems.

- Do not route USB 2.0 traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
- Separate signal traces into similar categories, and route similar signal traces together (such as routing differential-pairs together).
- Keep USB 2.0 signals clear of the core logic set. High current transients are produced during internal state transitions and can be very difficult to filter out.
- Follow the 20 x h rule by keeping traces at least [20 x (height above the plane)] mils away from the edge of the plane (VCC or GND). For an example stackup, the height above the plane is 4.5 mils (0.114 mm). This calculates to a 90-mil (2.286-mm) spacing requirement from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires and also helps prevent free radiation of the signal from the edge of the PCB.
- Avoid stubs on high-speed USB signals because stubs cause signal reflections and affect signal quality. If a stub is unavoidable in the design, the total of all the stubs on a particular line should not be greater than 200 mils (5.08 mm).

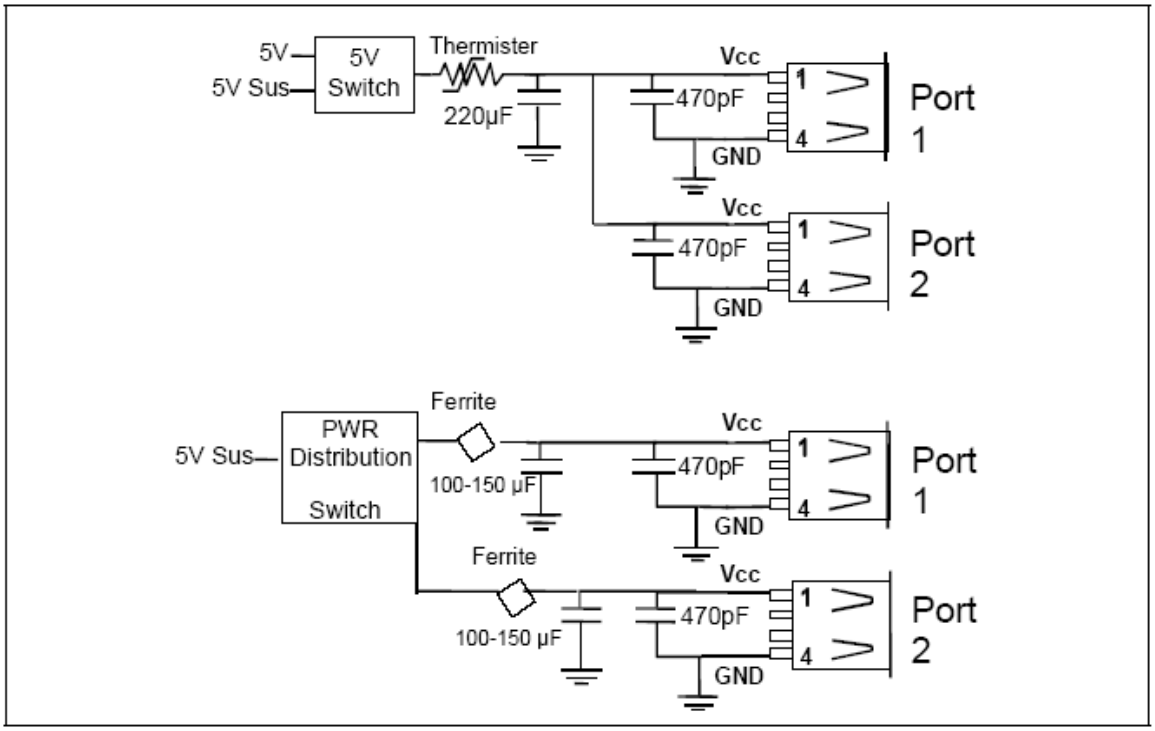
2.6.2.2 USB 2.0 Port Power Delivery

The following is a suggested topology for power distribution of VBUS to USB ports.

These circuits provide two types of protection during dynamic attach and detach situations on the bus: inrush current limiting (droop) and dynamic detach flyback protection. These two types require both bulk capacitance (droop) and filtering capacitance (for dynamic detach flyback voltage filtering). Intel recommends the following:

- Minimize the inductance and resistance between the coupling capacitors and the USB ports.
- Place capacitors as close as possible to the port and the power-carrying traces should be as wide as possible, preferably, a plane.
- Make the power-carrying traces wide enough that the system fuse blows on an over current event. If the system fuse is rated at 1 A, then the power-carrying traces should be wide enough to carry at least 1.5 A.

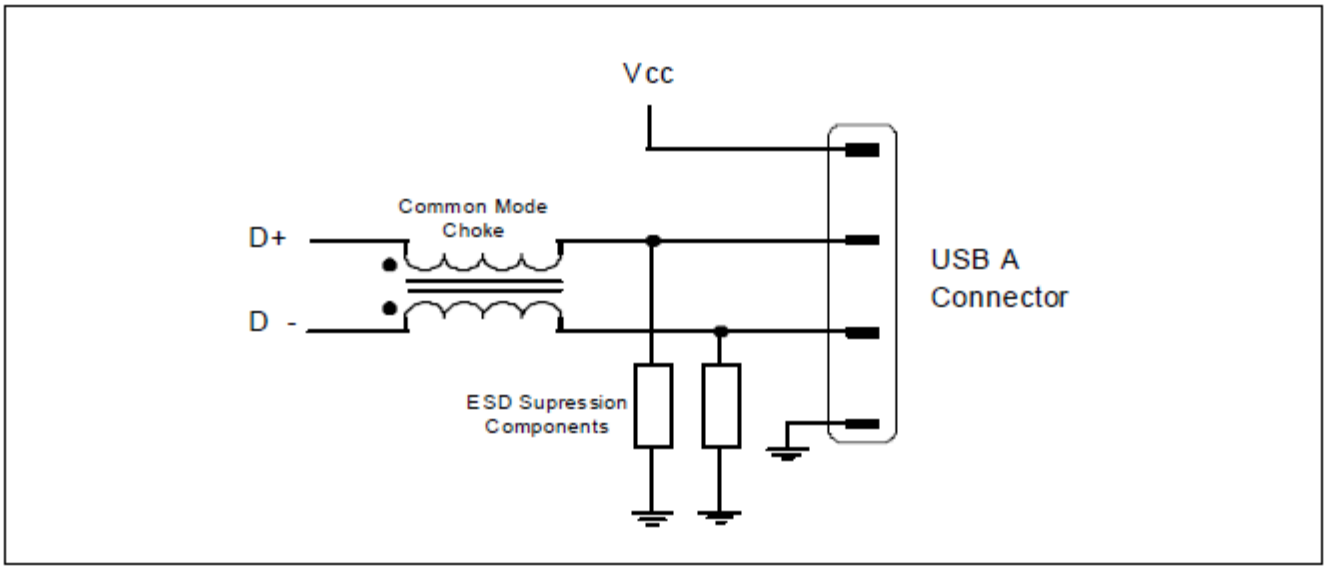
Figure 13: USB 2.0 Good Downstream Power Connection



2.6.2.3 USB 2.0 Common Mode Chokes

Testing has shown that common mode chokes can provide required noise attenuation. A design should include a common mode choke footprint to provide a stuffing option in the event the choke is needed to pass EMI testing. Below figure shows the schematic of a typical common mode choke and ESD suppression components. Place the choke as close as possible to the USB connector signal pins.

Figure 14: USB 2.0 A Common Mode Choke



Common mode chokes distort full-speed and high-speed signal quality. As the common mode impedance increases the distortion increases, therefore test the effects of the common mode choke on full speed and high-speed signal quality. Common mode chokes with a target impedance of 80 Ω to 90 Ω, at 100 MHz, generally provide adequate noise attenuation.

Finding a common mode choke that meets the designer's needs is a two-step process:

1. Choose a part with the impedance value that provides the required noise attenuation. This is a function of the electrical and mechanical characteristics of the part chosen and the frequency and strength of the noise present on the USB traces that should be suppressed.
2. After obtaining a part that gives passing EMI results, the second step is to test the effect this part has on signal quality. Higher impedance common mode chokes generally have a greater damaging effect on signal quality, so care must be used when increasing the impedance without doing thorough testing. Thorough testing means that the signal quality must be checked for low-speed, full-speed, and highspeed USB operation.

Further common mode choke information can be found on the high-speed USB Platform Design Guides available at www.usb.org.

2.6.2.4 EMI / ESD Protection

To improve the EMI behavior of the USB interface, a design should include common mode chokes, which have to be placed as close as possible to the USB connector signal pins.
Common mode chokes can provide required noise attenuation but they also distort the signal quality of full-speed and high-speed signaling. Therefore, common mode chokes should be chosen carefully to meet the requirements of the EMI noise filtering while retaining the integrity of the USB signals on the Carrier Board design.

To protect the USB host interface of the Module from over-voltage caused by electrostatic discharge (ESD) and electrical fast transients (EFT), low capacitance steering diodes and transient voltage suppression diodes have to be implemented on the Carrier Board design.

2.6.3 USB2.0 Trace Length Guidelines

Figure 15: Topology for USB2.0

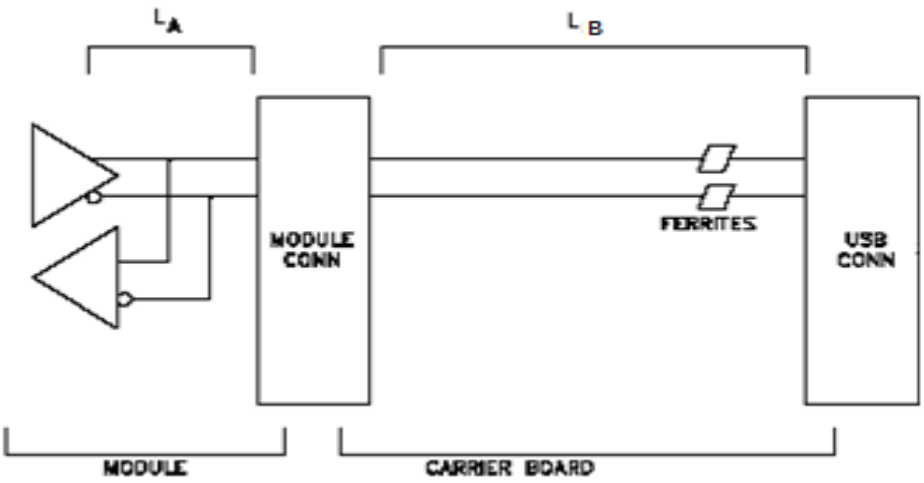


Table 18: USB2.0 Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	USB[7:0]+, USB[7:0]-	
Differential Impedance Target	85 Ω ±10%	
Single End	50Ω ±10%	
Spacing between pairs-to-pairs (inter-pair) (s)	Min. 20 mils	
Spacing between differential pairs and high-speed periodic Signals	Min. 50 mils	
Spacing between differential pairs and low-speed non periodic signals	Min. 20 mils	
LA	Please see the SOM-7569 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	12”	
Length matching	Differential pairs (intra-pair): Max. ±20 mils	
Reference Plane	GND referencing preferred	
Spacing from edge of plane	Min. 40mils	
Carrier Board Via Usage	Try to minimize number of vias	

Notes:

2.7 USB3.0

USB 3.0 is the third major revision of the Universal Serial Bus (USB) standard for computer connectivity. It adds a new transfer speed called SuperSpeed (SS) to the already existing LowSpeed (LS), FullSpeed (FS) and HighSpeed (HS).

USB 3.0 leverages the existing USB 2.0 infrastructure by adding two additional data pair lines to allow a transmission speed up to 5 Gbit/s, which is 10 times faster than USB 2.0 with 480 Mbit/s.

The additional data lines are unidirectional instead of the bidirectional USB 2.0 data lines. USB 3.0 is fully backward compatible to USB 2.0. USB 3.0 connectors are different from USB 2.0 connectors. The USB 3.0 connector is a super set of a USB 2.0 connector, with 4 additional pins that are invisible to USB 2.0 connectors. A USB 2.0 Type A plug may be used in a USB 3.0 Type A receptacle, but the USB 3.0 SuperSpeed functions will not be available.

2.7.1 USB3.0 Signal Definitions

Table 19: USB3.0 Signal Definitions

Signal	Pin#	Description	I/O	Note
USB_SSTX0+ USB_SSTX0-	B23 B22	USB Port 0, SuperSpeed TX + USB Port 0, SuperSpeed TX – Module has integrated AC Coupling Capacitors Carrier Board: Device - Connect to StdA_SSRX+/- Conn. - Connect 0Ω and 90Ω @100MHz USB3.0 Common Mode Choke(NL) combined in series and USB3.0 ESD suppressors to GND to Pin 9 StdA_SSTX+ / Pin 8 StdA_SSTX-, the value of CMC depends on EMI and signal integrity performance. N/C if not used	O PCIE	
USB_SSTX1+ USB_SSTX1-	B26 B25	USB Port 1, SuperSpeed TX + USB Port 1, SuperSpeed TX – Module has integrated AC Coupling Capacitors Carrier Board: Device - Connect to StdA_SSRX+/- Conn. - Connect 0Ω and 90Ω @100MHz USB3.0 Common Mode Choke(NL) combined in series and USB3.0 ESD suppressors to GND to Pin 9 StdA_SSTX+ / Pin 8 StdA_SSTX-, the value of CMC depends on EMI and signal integrity performance. N/C if not used	O PCIE	

Signal	Pin#	Description	I/O	Note
USB_SSRX0+ USB_SSRX0-	A23 A22	USB Port 0, SuperSpeed RX + USB Port 0, SuperSpeed RX – Carrier Board: Device - Connect AC Coupling Capacitors 100nF near COME to StdA_SSTX+/- Conn. - Connect 0Ω and 90Ω @100MHz USB3.0 Common Mode Choke(NL) combined in series and USB3.0 ESD suppressors to GND to Pin 6 StdA_SSRX+ / Pin 5 StdA_SSRX-, the value of CMC depends on EMI and signal integrity performance. N/C if not used	I PCIE	
USB_SSRX1+ USB_SSRX1-	A26 A25	USB Port 1, SuperSpeed RX + USB Port 1, SuperSpeed RX – Carrier Board: Device - Connect AC Coupling Capacitors 100nF near COME to StdA_SSTX+/- Conn. - Connect 0Ω and 90Ω @100MHz USB3.0 Common Mode Choke(NL) combined in series and USB3.0 ESD suppressors to GND to Pin 6 StdA_SSRX+ / Pin 5 StdA_SSRX-, the value of CMC depends on EMI and signal integrity performance. N/C if not used	I PCIE	

Notes:

2.7.1.1 USB Over-Current Protection (USB_x_y_OC#)

The USB Specification describes power distribution over the USB port, which supplies power for USB devices that are directly connected to the Carrier Board. Therefore, the host must implement over-current protection on the ports for safety reasons. Should the aggregate current drawn by the downstream ports exceed a permitted value, the over-current protection circuit removes power from all affected downstream ports. The over-current limiting mechanism must be resettable without user mechanical intervention. For more detailed information about this subject, refer to the 'Universal Serial Bus Specifications Revision 2.0', which can be found on the website http://www.usb.org.

Over-current protection for USB ports can be implemented by using power distribution switches on the Carrier Board that monitor the USB port power lines. Power distribution switches usually have a soft-start circuitry that minimizes inrush current in applications where highly capacitive loads are employed. Transient faults are internally filtered.

Additionally, they offer a fault status output that is asserted during over-current and thermal shutdown conditions. These outputs should be connected to the corresponding COM Express Modules USB over-current sense signals. Fault status signaling is an option at the USB specification. If you don't need the popup message in your OS you may leave the signals USB_0_1_OC#, USB_2_3_OC#, USB_4_5_OC# and USB_6_7_OC# unconnected.

Fault status signals are connected by a pullup resistor to VCC_3V3_SBY on COM Express Module. Please check your tolerance on a USB port with VCC_5V supply.

USB 2.0 port's VCC current limit should be set to 500mA. For USB 3.0 implementations, the VCC current limit is raised to 1A. A different, USB 3.0 compatible, power switch is used.

2.7.1.2 EMI / ESD Protection

To improve the EMI behavior of the USB interface, a design should include common mode chokes, which have to be placed as close as possible to the USB connector signal pins.

Common mode chokes can provide required noise attenuation but they also distort the signal quality of FullSpeed, HighSpeed and SuperSpeed signaling. Therefore, common mode chokes should be chosen carefully to meet the requirements of the EMI noise filtering while retaining the integrity of the USB signals on the Carrier Board design.

To protect the USB host interface of the Module from over-voltage caused by electrostatic discharge (ESD) and electrical fast transients (EFT), low capacitance steering diodes and transient voltage suppression diodes have to be implemented on the Carrier Board design.

2.7.2 USB3.0 Routing Guidelines

USB3.0 Insertion Loss Budget

Figure 16: USB3.0 Insertion Loss Budget

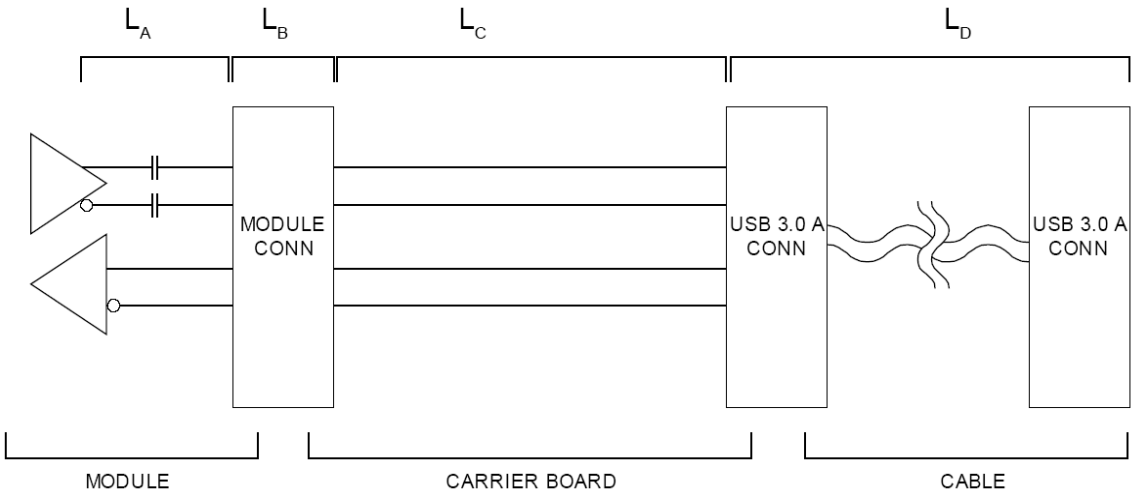


Table 20: USB3.0 Insertion Loss Budget

Segment	Loss (dB)	Notes
L_A	1.94	Up to 3 inches of Module trace @ 2.5 GHz
L_B	1.20	COM Express connector at 2.5 GHz
L_C	3.64	Up to 5 inches of Carrier Board trace @ 2.5 GHz with Common-Mode Component
Total	6.78	

COM ExpressTM USB implementations should conform to insertion loss values less than or equal to those shown in the table above. The insertion loss values shown account for frequency dependent material losses only. Cross talk losses are separate from material losses in the USB specification.

"Device Down" implementations, in which the USB target device is implemented on the Carrier Board, may add the ferrite and USB connector insertion loss values to the Carrier Board budget.

The Carrier Board insertion loss budget then becomes LC + LD, or 2.68 dB.

2.7.2.1 USB3.0 Differential Transitional Via Recommendations

Please refer to 2.3.4.3

2.7.3 USB3.0 Trace Length Guidelines

Figure 17: Topology for USB3.0

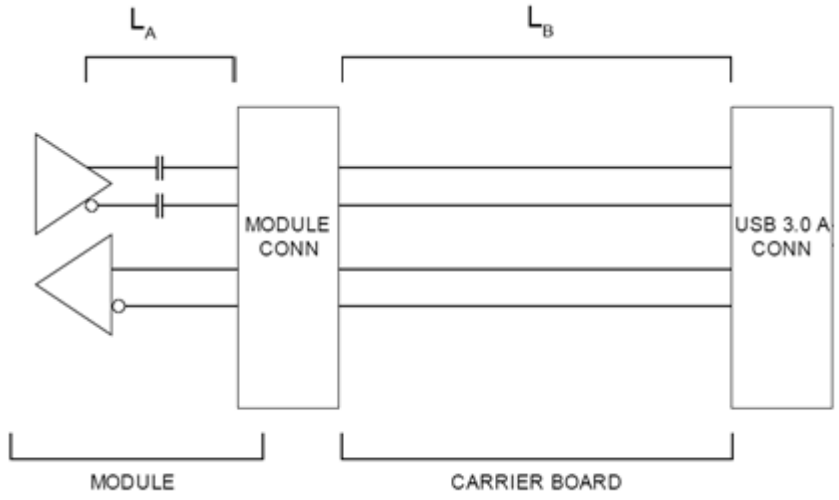


Table 21: USB3.0 Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	USB3.0	
Differential Impedance Target	85 Ω ±10%	
Single End	50Ω ±10%	
Spacing between pairs-to-pairs (inter-pair) (s)	Min. 15 mils	
Spacing between differential pairs and high-speed periodic Signals	Min. 15 mils	
Spacing between differential pairs and low-speed non periodic signals	Min. 20 mils	
LA	Please see the SOM-7569 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	8”	
Length matching	Differential pairs (intra-pair): Max. ±15 mils	
Reference Plane	GND referencing preferred	
Spacing from edge of plane	Min. 40mils	
Carrier Board Via Usage	Max. 3 vias per differential signal trace	

Notes:

2.8 SATA

Support for up to four SATA ports is defined on the COM Express A-B connector. Support for a minimum of one port is required for Module Type10. The COM Express Specification allows for both SATA-150 and SATA-300 implementations. Constraints for SATA-300 implementations are more severe than those for SATA-150. The COM Express Specification addresses both in the section on insertion losses.

SATA devices can be internal to the system or external. The eSATA specification defines the connector used for external SATA devices. The eSATA interface must be designed to prevent damage from ESD, comply with EMI limits, and withstand more insertion/removals cycles than standard SATA. A specific eSATA connector was designed to meet these needs. The Esata connector does not have the "L" shaped key, and because of this, SATA and eSATA cables cannot be interchanged.

2.8.1 SATA Signal Definitions

Table 22: SATA Signal Definitions

Signal	Pin#	Description	I/O	Note
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0, Receive input differential pair. Module has integrated AC Coupling capacitor Carrier Board: Connect to SATA0 Conn pin 6 RX+ Connect to SATA0 Conn pin 5 RX- N/C if not used.	I SATA	
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0, Transmit output differential pair. Module has integrated AC Coupling capacito Carrier Board: Connect to SATA0 Conn pin 2 TX+ Connect to SATA0 Conn pin 3 TX- N/C if not used.	O SATA	
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1, Receive input differential pair. Module has integrated AC Coupling capacitor Carrier Board: Connect to SATA1 Conn pin 6 RX+ Connect to SATA1 Conn pin 5 RX- N/C if not used.	I SATA	

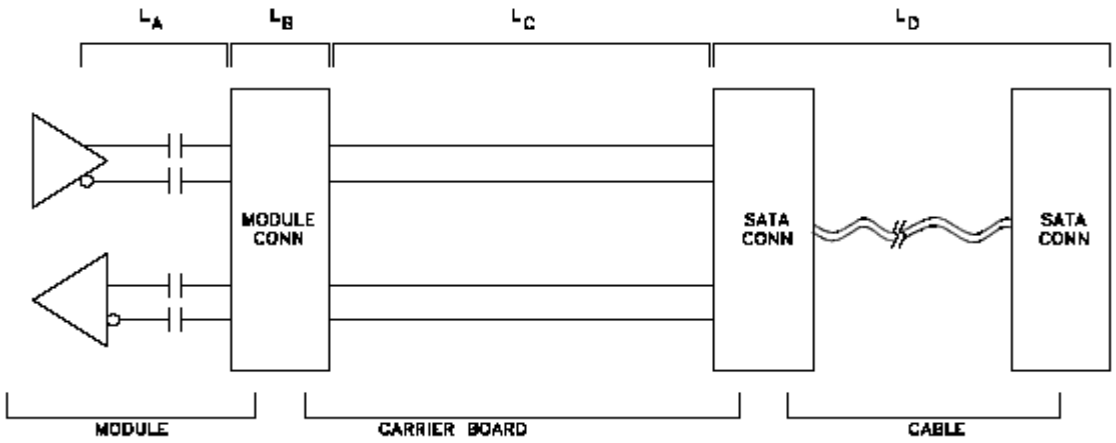
Signal	Pin#	Description	I/O	Note
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1, Transmit output differential pair. Module has integrated AC Coupling capacito Carrier Board: Connect to SATA1 Conn pin 2 TX+ Connect to SATA1 Conn pin 3 TX- N/C if not used.	O SATA	
SATA_ACT#	A28	Serial ATA activity LED. Open collector output pin driven during SATA command activity. Module has integrated PU resistor Carrier Board: Connect to LED and current limiting resistors 250 to 330 Ω to 3.3V N/C if not used.	O 3.3V CMOS OC	Able to drive 10 mA

Notes:

2.8.2 SATA Routing Guidelines

SATA Insertion Loss Budget

Figure 18: SATA Insertion Loss Budge



The Serial ATA source specification provides insertion loss figures only for the SATA cable. There are several cable types defined with insertion losses ranging from 6 dB up to 16 dB. Cross talk losses are separate from material losses in the SATA specification.

The COM ExpressTM SATA Insertion loss budgets presented below represent the material losses and do not include cross talk losses. The COM ExpressTM SATA Insertion loss budgets are a guideline: module and Carrier Board vendors should not exceed the values shown in the tables below.

Table 23: SATA Insertion Loss Budge

SATA Gen 1 Insertion Loss Budget, 1.5 GHz

Segment	Loss (dB)	Notes
L_A	1.26	Up to 3.0 inches of module trace @ 0.28 dB / GHz / inch
Coupling Caps	0.40	
L_B	0.25	COM Express™ connector at 1.5 GHz measured value
L_C	3.07	Up to 7.2 inches of Carrier Board trace @ 0.28 dB / GHz / inch
L_D	6.00	Source specification cable and cable connector allowance
Total	10.98	

SATA Gen 2 Insertion Loss Budget, 3.0 GHz

Segment	Loss (dB)	Notes
L_A	1.68	Up to 2.0 inches of module trace @ 0.28 dB / GHz / inch
Coupling Caps	0.40	
L_B	0.38	COM Express™ connector at 3.0 GHz measured value
L_C	2.52	Up to 3.0 inches of Carrier Board trace @ 0.28 dB / GHz / inch
L_D	6.00	Source specification cable and cable connector allowance
Total	10.98	

2.8.2.1 General SATA Routing Guidelines

Use the following general routing and placement guidelines when laying out a new design.

- SATA signals must be ground referenced. If changing reference plane is completely unavoidable (that is, ground reference to power reference), proper placement of stitching caps can minimize the adverse effects of EMI and signal quality performance caused by reference plane change. Stitching capacitors are smallvalued capacitors (1 µF or lower in value) that bridge the power and ground planes close to where a high-speed signal changes layers. Stitching caps provide a high frequency current return path between different reference planes. They minimize the impedance discontinuity and current loop area that crossing different reference planes created. The maximum number allowed for SATA to change reference plane is one.
- Route all traces over continuous GND planes, with no interruptions. Avoid crossing over anti-etch if at all possible. Any discontinuity or split in the ground plane can cause signal reflections and should be avoided.
- Minimize layer changes. If a layer change is necessary, ensure that trace matching for either transmit or receive pair occurs within the same layer. Intel recommends to use SATA vias as seldom as possible.
- **DO NOT** route SATA traces under power connectors, other interface connectors, crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
- **DO NOT** place stubs, test points, test vias on the route to minimize reflection. Utilize vias and connector pads as test points instead.
- For testability, route the TX and RX pairs for a given port on the same layer and close to each other to help ensure that the pairs share similar signaling characteristics. If the groups of traces are similar, a measure of RX pair layout quality can be approximated by using the results from actively testing the TX pair's signal quality.
- Length matching rules are required on SATA differential signals for optimum timing margins, preventing common-mode signals and EMI.Each net within a differentialpair should be length matched on a segment-by-segment basis at the point of discontinuity. Total length mismatch must not be more than 20 mils (0.508 mm). Examples of segments might include breakout areas, routes running between two vias, routes between an AC coupling capacitor and a connector pin, etc. The points of discontinuity would be the via, the capacitor pad, or the connector pin.Matching of TX and RX within the same port and between SATA TX and RX pairs from differential ports is not required. When length matching compensation occurs, it should be made as close as possible to the point where the variation occurs.
- **DO NOT** serpentine to match RX and TX traces; there is **NO** requirement to match RX and TX traces. In addition, **DO NOT** serpentine to meet minimum length guidelines on RX and TX traces.
- Recommend keeping SATA traces 20 mils (0.508 mm) from any vias on the motherboard whenever possible.

2.8.2.2 SATA Differential Transitional Via Recommendations

Please refer to 2.3.4.3

2.8.3 SATA Trace Length Guidelines

Figure 19: Topology for SATA

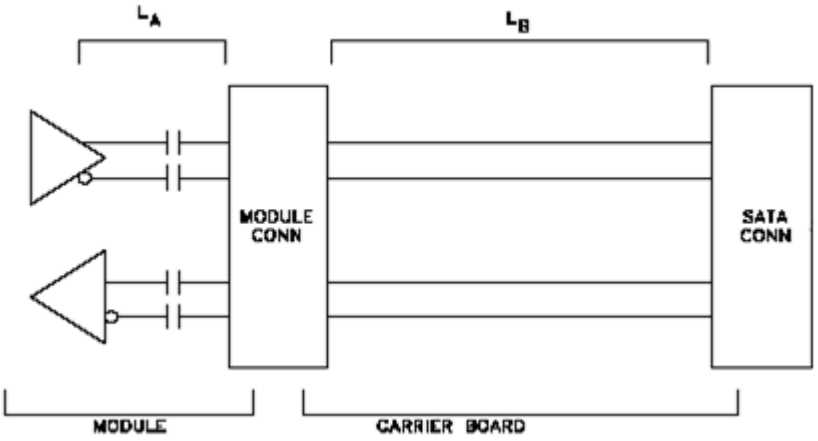


Table 24: SATA Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	SATA	
Differential Impedance Target	85 Ω ±10%	
Single End	50Ω ±10%	
Signal length available for the COM Express Carrier Board	3 inches, a redriver may be necessary for GEN3 signaling rates	
Spacing between RX and TX pairs (inter-pair) (s)	Min. 20 mils	
Spacing between differential pairs and high-speed periodic Signals	Min. 50 mils	
Spacing between differential pairs and low-speed non periodic signals	Min. 20 mils	
LA	Please see the SOM-7569 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	5.5”	
Length matching	Differential pairs (intra-pair): Max. ±5 mils	
Reference Plane	GND referencing preferred	
Spacing from edge of plane	Min. 40mils	
Carrier Board Via Usage	A maximum of 2 vias is recommended.	

Notes:

2.9 LVDS

2.9.1 Signal Definitions

The COM Express Specification provides an optional LVDS interface on the COM Express A-B connector.

Systems use a single-channel LVDS for most displays. Single-channel LVDS means that one complete RGB pixel is transmitted per display input clock.

Each COM Express LVDS channel consists of four differential data pairs and a differential clock pair for a total of five differential pairs per channel. COM Express Modules and Module chipsets may not use all pairs. For example, with 18-bit TFT displays, only three of the four data pairs on the LVDS_A channel are used, along with the LVDS_A clock. The manner in which RGB data is packed onto the LVDS pairs (including packing order and color depth) is not specified by the COM Express Specification. This may be Module-dependent.

There are five single-ended signals included to support the LVDS interface: two lines are used for an I2C interface that may be used to support EDID or other panel information and identification schemes. Additionally, there are an LVDS power enable (LVDS_VDD_EN) and backlight control and enable lines (LVDS_BKLT_CTRL and LVDS_BKLT_EN).

Table 25: LVDS Signal Definitions

Signal	Pin#	Description	I/O	Note
LVDS_A0+ LVDS_A0-	A71 A72	LVDS channel A differential signal pair 0 Carrier Board: Connect 100Ω @100MHz Common Choke in series to Reciever - RXinO0+/- with 100Ω termination Conn. - RXinO0+/- N/C if not used	O LVDS	
LVDS_A1+ LVDS_A1-	A73 A74	LVDS channel A differential signal pair 1 Carrier Board: Connect 100Ω @100MHz Common Choke in series to Reciever – RxinO1+/- with 100Ω termination Conn. – RxinO1+/- N/C if not used	O LVDS	

Signal	Pin#	Description	I/O	Note
LVDS_A2+ LVDS_A2-	A75 A76	LVDS channel A differential signal pair 2 Carrier Board: Connect 100Ω @100MHz Common Choke in series to Reciever – RxinO2+/- with 100Ω termination Conn. – RxinO2+/- N/C if not used	O LVDS	
LVDS_A3+ LVDS_A3-	A78 A79	LVDS channel A differential signal pair 3 Carrier Board: Connect 100Ω @100MHz Common Choke in series to Reciever – RxinO3+/- with 100Ω termination Conn. – RxinO3+/- N/C if not used	O LVDS	
LVDS_A_CK+ LVDS_A_CK-	A81 A82	LVDS channel A differential clock pair Carrier Board: Connect 100Ω @100MHz Common Choke in series to Reciever - RXOC+/- with 100Ω termination Conn. - RXOC+/- N/C if not use	O LVDS	
LVDS_VDD_EN	A77	LVDS flat panel power enable. Carrier Board: Connect to enable control of LVDS panel power circuit. N/C if not used	O 3.3V, CMOS	
LVDS_BKLT_EN	B79	LVDS flat panel backlight enable high active signal Carrier Board: Connect to enable control of LVDS panel backlight power circuit. N/C if not used	O 3.3V, CMOS	
LVDS_BKLT_CTRL	B83	LVDS flat panel backlight brightness control Carrier Board: Connect to brightness control of LVDS panel backlight power circuit. N/C if not used	O 3.3V, CMOS	
LVDS_I2C_CK	A83	DDC I2C clock signal used for flat panel detection and control. Carrier Board: Connect to DDC clock of LVDS panel N/C if not used	O 3.3V, CMOS	
LVDS_I2C_DAT	A84	DDC I2C data signal used for flat panel detection and control. Carrier Board: Connect to DDC data of LVDS panel N/C if not used	I/O 3.3V, OD CMOS	

2.9.1.1 Display Timing Configuration

The graphic controller needs to be configured to match the timing parameters of the attached flat panel display. To properly configure the controller, there needs to be some method to determine the display parameters. Different Module vendors provide differing ways to access display timing parameters. Some vendors store the data in non-volatile memory with the BIOS setup screen as the method for entering the data, other vendors might use a Module or Carrier based EEPROM. Some vendors might hard code the information into the BIOS, and other vendors might support panel located timing via the signals LVDS_I2C_CK and LVDS_I2C_DAT with an EEPROM strapped to 1010 000x. Regardless of the method used to store the panel timing parameters, the video BIOS will need to have the ability to access and decode the parameters. Given the number of variables it is recommended that Carrier designers contact Module suppliers to determine the recommend method to store and retrieve the display timing parameters.

The Video Electronics Standards Association (VESA) recently released DisplayID, a second generation display identification standard that can replace EDID and other proprietary methods for storing flat panel timing data. DisplayID defines a data structure which contains information such as display model, identification information, colorimetry, feature support, and supported timings and formats. The DisplayID data allows the video controller to be configured for optimal support for the attached display without user intervention. The basic data structure is a variable length block up to 256 bytes with additional 256 byte extensions as required. The DisplayID data is typically stored in a serial EPROM connected to the LVDS_I2C bus. The EPROM can reside on the display or Carrier. DisplayID is not backwards compatible with EDID. Contact VESA (www.vesa.org) for more information.

2.9.1.2 Backlight Control

Backlight inverters are either voltage, PWM or resistor controlled. The COM Express specification provides two methods for controlling the brightness. One method is to use the backlight control and enable signals from the CPU chipset. These signals are brought on COM Express LVDS_BKLT_EN and LVDS_BKLT_CTRL. LVDS_BKLT_CTRL is a Pulse Width Modulated (PWM) output that can be connected to display inverters that accept a PWM input. The second method it to use the LVDS I2C bus to control an I2C DAC. The output of the DAC can be used to support voltage controlled inverters. The DAC can be used driving the backlight voltage control input pin of the inverter.

2.9.2 LVDS Routing Guidelines

Route LVDS signals as differential pairs (excluding the five single-ended support signals), with a 100-Ω differential impedance and a 55-Ω, single-ended impedance. Ideally, a LVDS pair is routed on a single layer adjacent to a ground plane. LVDS pairs should not cross plane splits. Keep layer transitions to a minimum. Reference LVDS pairs to a power plane if necessary. The power plane should be well-bypassed.

Length-matching between the two lines that make up an LVDS pair (“intra-pair”) and between different LVDS pairs (“inter-pair”) is required. Intra-pair matching is tighter than the inter-pair matching.
All LVDS pairs should have the same environment, including the same reference plane and the same number of vias.

2.9.3 LVDS Trace Length Guidelines

Figure 20: Topology for LVDS

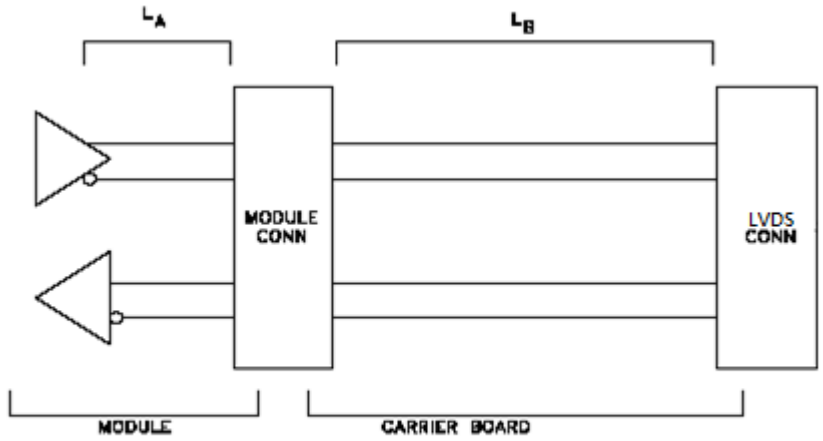


Table 26: LVDS Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	LVDS	
Differential Impedance Target	85 Ω ±10%	
Single End	50Ω ±10%	
Signal length to the LVDS connector available for the COM Express Carrier Board	4”	
Spacing between pair to pairs (inter-pair) (s)	Min. 20 mils	
Spacing between differential pairs and high-speed periodic signals	Min. 30 mils	
Spacing between differential pairs and low-speed non periodic signals	Min. 20 mils	
LA	Please see the SOM-7569 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	4”	
Length matching	Differential pairs (intra-pair): Max. 5 mils Clock and data pairs (intra-pair): Max. 100 mils data pairs (inter-pair) : Max. 100 mils	
Reference Plane	GND referencing preferred	
Spacing from edge of plane	Min. 40mils	
Carrier Board Via Usage	Max. of 2 vias per line.	

Notes:

2.10 Embedded DisplayPort (eDP)

Embedded DisplayPort (eDP) is a digital display interface standard produced by the Video Electronics Standards Association (VESA) for digital interconnect of Audio and Video.

Embedded DisplayPort defines a standardized display panel interface for internal connections; e.g., graphics interfaces to notebook display panels. It supports advanced power-saving features including seamless refresh rate switching, display panel and backlight control protocol that works through the AUX channel, and Panel Self-Refresh (PSR) feature developed to save system power and further extend battery life in portable PC systems. PSR mode allows the GPU to enter power saving states in between frame updates by including framebuffer memory in the display panel controller.

Embedded DisplayPort is intended to replace LVDS as the interface to flat panel displays integrated into a product. Unlike DisplayPort, embedded DisplayPort does not define a specific connector or pin-out. The COM Express specification shares the LVDS pins with embedded DisplayPort.

2.10.1 eDP Signal Definitions

eDP is available in Type 6 and type 10 pin-outs as an alternative to the LVDS A channel. The Module can provide LVDS only, eDP only or Dual-Mode for both interfaces. Please refer to relevant Module documentation for the supported interfaces.

Table 27: eDP Signal Definitions

Signal	Pin#	Description	I/O	Note
eDP_TX0+ eDP_TX0-	A75 A76	eDP lane 0, TX +/- Carrier Board: Connect AC Coupling Capacitors 75~200 nF near eDP connector. N/C if not used	O PCIe	1
eDP_TX1+ eDP_TX1-	A73 A74	eDP lane 1, TX +/- Carrier Board: Connect AC Coupling Capacitors 75~200 nF near eDP connector. N/C if not used	O PCIe	1
eDP_TX2+ eDP_TX2-	A71 A72	eDP lane 2, TX +/- Carrier Board: Connect AC Coupling Capacitors 75~200 nF near eDP connector. N/C if not used	O PCIe	1

Signal	Pin#	Description	I/O	Note
eDP_TX3+ eDP_TX3-	A81 A82	eDP lane 3, TX +/- Carrier Board: Connect AC Coupling Capacitors 75~200 nF near eDP connector. N/C if not used	O PCIe	1
eDP_VDD_EN	A77	eDP power enable Carrier Board: Connect to enable control of eDP panel power circuit. N/C if not used	O CMOS	1
eDP_BLKT_EN	B79	eDP backlight enable Carrier Board: Connect to enable control of eDP panel backlight power circuit. N/C if not used	O CMOS	1
eDP_BLKT_CTRL	B83	EDP backlight brightness control Carrier Board: Connect to brightness control of eDP panel backlight power circuit. N/C if not used	O CMOS	1
eDP_AUX+ eDP_AUX-	A83 A84	eDP auxiliary lane +/- Carrier Board: Connect AC Coupling Capacitors 100 nF near eDP connector. N/C if not used.	I/O PCIe	1
eDP_HPD	A87	Detection of Hot Plug / Unplug and notification of the link layer Carrier Board: Connector to device or eDP connector HP pin.	I CMOS	1

Notes:

1. SOM-7569 default is LVDS. BOM option with eDP.

2.10.2 eDP Trace Length Guidelines

Figure 21: Topology for eDP

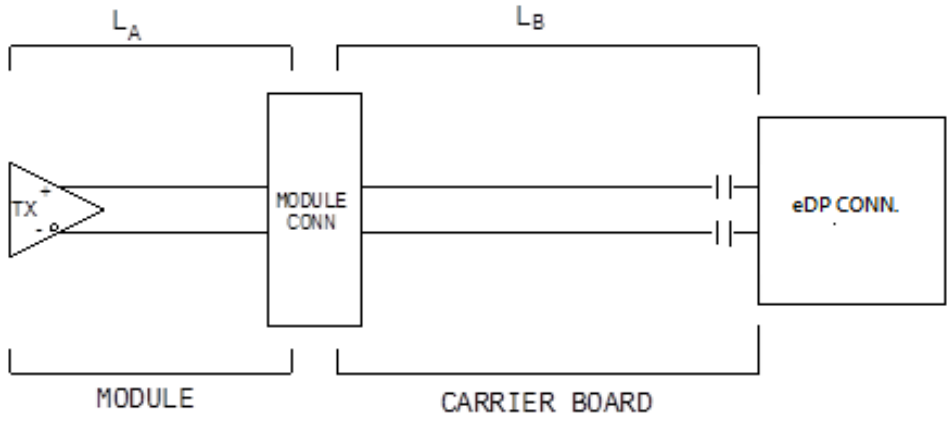


Table 28: DisplayPort Connector / Device Down Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	eDP	
Differential Impedance Target	85 Ω ±10%	
Single End	50Ω ±10%	
Isolation to equivalent pairs	20 mils (MS) and 15 mils (DS)	
Isolation to other signal groups	20 mils (MS) and 15 mils (DS)	
LA	SOM-7569 don't support eDP by default	
LB	Carrier Board Length	
Max length of LA+LB	eDP differential pairs to eDP connector: 10" AUX channel: 10"	
Length matching	Differential pairs (intra-pair): Max. 5 mils For each channel, match the lengths of the differential pairs (Inter-Pair) to be within a 1-inch window (max length – min length < 1 inch (2.54 cm)).	
Reference Plane	GND referencing preferred. Min 40-mil trace edge-to-major plane edge spacing.	
Carrier Board Via Usage	Max. 2 vias.	
AC coupling	Min = 75 nF Max = 200 nF	1

Notes:

1. AC caps are recommended to be placed close to device side (avoid placing AC cpas on mid-bus).
2. SOM-7569 don't support eDP by default, it is option function. If customers want to use eDP function, please contact Advantech.

2.11 Digital Audio Interfaces

The COM Express Specification allocates seven pins on the A-B connector to support digital AC'97 and HD interfaces to audio Codecs on the Carrier Board. The pins are available on all Module types. High-definition (HD) audio uses the same digital-signal interface as AC '97 audio. Codecs for AC '97 and HD Audio are different and not compatible. Current Module chipsets support HD Audio only.

2.11.1 Audio Codec Signal Descriptions

Table 29: Audio Codec Signal Descriptions

Signal	Pin#	Description	I/O	Note
AC/HDA_RST#	A30	CODEC Reset. Carrier Board: AC97 - Connect 0 Ω in series to CODEC pin 11 RESET# HDA - Connect 0 Ω in series to CODEC pin 11 RESET# N/C if not used	O 3.3V Suspend CMOS	
AC/HDA_SYNC	A29	Serial Sample Rate Synchronization. Carrier Board: AC97 - Connect 0 Ω in series to CODEC pin 10 SYNC HDA - Connect 0 Ω in series to CODEC pin 10 SYNC N/C if not used	O 3.3V CMOS	
AC/HDA_BITCLK	A32	24 MHz Serial Bit Clock for HDA CODEC. Carrier Board: AC97 - Connect 33-47 Ω in series to CODEC pin 6 BIT_CLK HDA - Module has integrated series resistor. Connect 0 Ω in series to CODEC pin 6 BIT_CLK N/C if not used	O 3.3V CMOS	
AC/HDA_SDOUT	A33	Audio Serial Data Output Stream. Carrier Board: AC97 - Connect 33-47 Ω in series to CODEC pin 5 SDATA_OUT HDA - Connect 33-47 Ω in series and PD 10KΩ(NL) to CODEC pin 5 SDATA_OUT N/C if not used	O 3.3V CMOS	
AC/HDA_SDIN0 AC/HDA_SDIN1 AC/HDA_SDIN2	B30 B29 B28	Audio Serial Data Input Stream from CODEC[0:2]. Carrier Board: AC97 - Connect 33-47 Ω in series to CODEC pin 8 SDATA_IN HDA - Connect 33-47 Ω in series and PD 10KΩ(NL) to CODEC pin 8 SDATA_IN N/C if not used	I 3.3V Suspend CMOS	

The codec on a COM Express Carrier Board is usually connected as the primary codec with the codec ID 00 using the data input line 'AC/HDA_SDIN0'. Up to two additional codecs with ID 01 and ID 10 can be connected to the COM Express Module by using the other designated signals 'AC/HDA_SDIN1' and 'AC/HDA_SDIN2'.

Connect the primary audio codec to the serial data input signal 'AC/HDA_SDIN0' and ensure that the corresponding bit clock input signal 'AC/HDA_BITCLK' is connected to the AC'97/HDA interface of the COM Express Module.

Clocking over the signal 'AC/HDA_BITCLK' is derived from a 24.576 MHz crystal or crystal oscillator provided by the primary codec in AC97 implementations. The crystal is not required in HDA implementations. This clock also drives the second and the third audio codec if more than one codec is used in the application. For crystal or crystal oscillator requirements, refer to the datasheet of the primary codec.

2.11.2 Audio Routing Guidelines

The implementation of proper component placement and routing techniques will help to ensure that the maximum performance available from the codec is achieved. Routing techniques that should be observed include properly isolating the codec, associated audio circuitry, analog power supplies and analog ground planes from the rest of the Carrier Board. This includes split planes and the proper routing of signals not associated with the audio section.

The following is a list of basic recommendations:
Traces must be routed with a target impedance of 50Ω with an allowed tolerance of ±15%.
Ground return paths for the analog signals must be given special consideration.
Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines.
Locate the analog and digital signals as far as possible from each other.
Partition the Carrier Board with all analog components grouped together in one area and all digital components in another.
Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
Provide separate analog and digital ground planes with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between the planes must be a minimum of 0.05 inch wide.
Route analog power and signal traces over the analog ground plane.
Route digital power and signal traces over the digital ground plane.
Position the bypassing and decoupling capacitors close to the IC pins with wide traces to reduce impedance.
Place the crystal or oscillator (depending on the codec used) as close as possible to the codec. (HDA implementations generally do not require a crystal at the codec)
Do not completely isolate the analog/audio ground plane from the rest of the Carrier Board ground plane. Provide a single point (0.25 inch to 0.5 inch wide) where the analog/isolated ground plane connects to the main ground plane. The split between the planes must be a minimum of 0.05 inch wide.
Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main Carrier Board ground. That is, no signal should cross the split/gap between the ground planes, because this would cause a ground loop, which in turn would greatly increase EMI emissions and degrade the analog and digital signal quality.

2.11.3 Audio Trace Length Guidelines

Figure 22: Topology for Audio

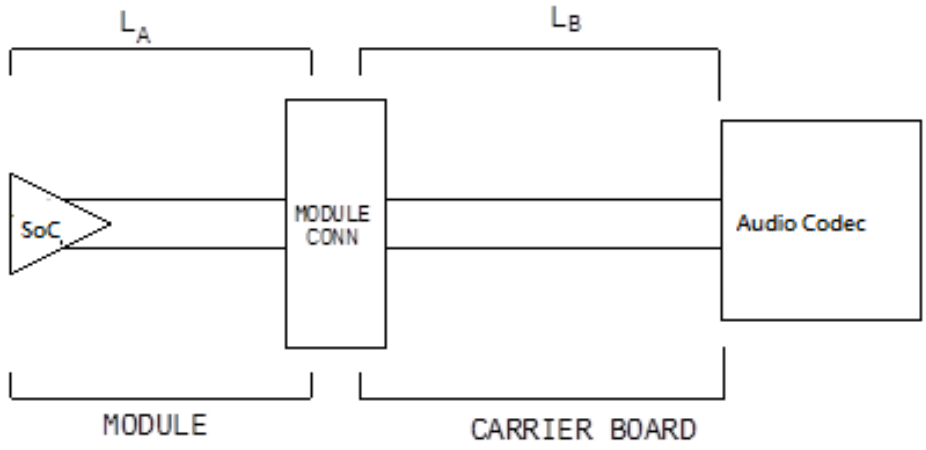


Table 30: Audio Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	Audio	
Single End	50Ω ±10%	
Nominal Trace Space within Audio Signal Group	Min. 15mils	
Spacing to Other Signal Group	Min. 20mils	
LA	Please see the SOM-7569 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	14”	
Length matching	Data to Clock must be matched within 500mils	
Reference Plane	GND referencing preferred. Min 20-mil trace edge-to-major plane edge spacing.	

Notes:

2.12 LPC Bus – Low Pin Count Interface

Since COM Express is designed to be a legacy free standard for embedded Modules, it does not support legacy functionality on the Module, such as PS/2 keyboard/mouse, serial ports, and parallel ports. Instead, it provides an LPC interface that can be used to add peripheral devices to the Carrier Board design. COM Express also provides interface pins necessary for (optional) Carrier Board resident PS keyboard controllers.

The Low Pin Count Interface was defined by the Intel® Corporation to facilitate the industry's transition toward legacy free systems. It allows the integration of low-bandwidth legacy I/O components within the system, which are typically provided by a Super I/O controller. Furthermore, it can be used to interface Firmware Hubs, Trusted Platform Module (TPM) devices, general-purpose inputs and outputs, and Embedded Controller solutions. Data transfer on the LPC bus is implemented over a 4 bit serialized data interface, which uses a 24MHzz LPC bus clock. It is straightforward to develop PLDs or FPGAs that interface to the LPC bus.

For more information about LPC bus, refer to the 'Intel Low Pin Count Interface Specification Revision 1.1'.

2.12.1 LPC Signal Definition

Table 31: LPC Interface Signal Definition

Signal	Pin#	Description	I/O	Note
LPC_SERIRQ	A50	LPC serialized IRQ. Carrier Board: Connect to LPC - SERIRQ N/C if not use	I/O 3.3V CMOS	
LPC_FRAME#	B3	LPC frame indicates start of a new cycle or termination of a broken cycle. Carrier Board: LPC - LFRAME# FWH - Pin 23 LFRAME# N/C if not used	O 3.3V CMOS	

Signal	Pin#	Description	I/O	Note
LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3	B4 B5 B6 B7	LPC multiplexed command, address and data. Carrier Board: Connect to LPC - LAD0 , LAD1, LAD2, LAD3 FWH - Pin 13 LAD0, Pin 14 LAD1, Pin 15 LAD2, Pin 17 LAD3 N/C if not used	I/O 3.3V CMOS	
LPC_DRQ0# LPC_DRQ1#	B8 B9	LPC encoded DMA/Bus master request. Carrier Board: Connect to LPC - LDRQ0#, LDRQ1# N/C if not used	I 3.3V CMOS	Not all Modules support LPC DMA. Contact your vendor for information
LPC_CLK	B10	LPC clock output 24MHzz. Carrier Board: Connect to LPC - LCLK FWH - Pin 31 LCLK N/C if not used	O 3.3V CMOS	

Note

Implementing external LPC devices on the COM Express Carrier Board always requires customization of the COM Express Module's BIOS in order to support basic initialization for those LPC devices. Otherwise the functionality of the LPC devices will not be supported by a Plug&Play or ACPI capable system.

2.12.2 LPC Routing Guidelines

2.12.2.1 General Signals

LPC signals are similar to PCI signals and may be treated similarly. Route the LPC bus as 50 Ω, single-ended signals. The bus may be referenced to ground (preferred), or to a well-bypassed power plane or a combination of the two. Point-to-point (daisy-chain) routing is preferred, although stubs up to 1.5 inches may be acceptable. Length-matching among LPC_AD[3:0], LPC_FRAME# are needed

2.12.2.2 Bus Clock Routing

Route the LPC clock as a single-ended, 50 Ω trace with generous clearance to other traces and to itself. A continuous ground-plane reference is recommended. Routing the clock on a single ground referenced internal layer is preferred to reduce EMI.

The LPC clock implementation should follow the routing guidelines for the PCI clock defined in the COM Express specification and the 'PCI Local Bus Specification Revision 2.3'.

2.12.3 LPC Trace Length Guidelines

Figure 23: Topology for LPC

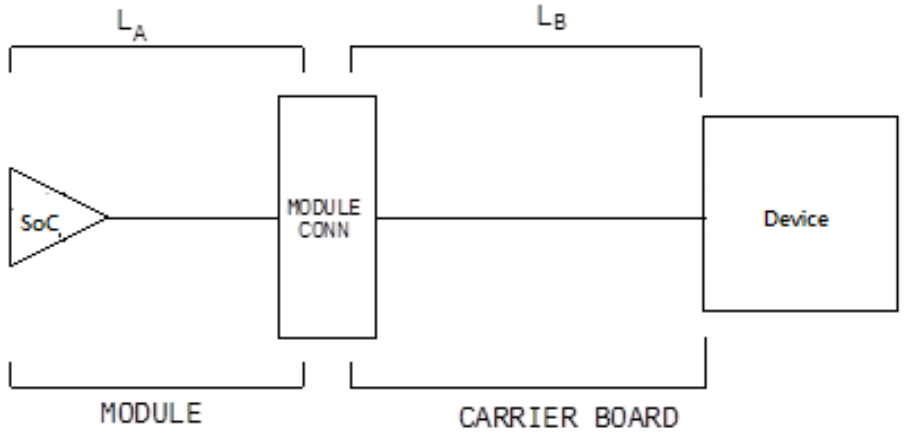


Table 32: LPC Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	LPC	
Single End	50Ω ±10%	
Nominal Trace Space within LPC Signal Group	Min. 15mils	
Spacing to Other Signal Group	Min. 15mils	
LA	Please see the SOM-7569 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	13”	
Length matching between single ended signals	Max. 500mils	
Length matching between clock signals	Max. 500mils	
Reference Plane	GND referencing preferred.	
Via Usage	Try to minimize number of vias	

Notes:

2.13 SPI – Serial Peripheral Interface Bus

The SPI interface is defined in this specification to service as an off-module option for BIOS storage. The SPI interface replaces the LPC Firmware Hub interface, which is now considered a legacy interface for firmware storage (LPC does continue to be used for SuperIO connectivity).

Many current chipsets only specify SPI for BIOS/Firmware storage usage, so the COM.0 specification is limited to that connectivity use-case to enable maximum compatibility across Modules and silicon platforms. Additional features, such as SPI-based Trusted Platform Module support might be added to a given carrier design, but compatibility is not guaranteed across Modules.

2.13.1 SPI Signal Definition

Table 33: SPI Interface Signal Definition

Signal	Pin#	Description	I/O	Note
SPI_CS#	B97	Chip select for Carrier Board SPI – may be sourced from chipset SPI0 or SPI1 Carrier Board: Connect to SPI flash pin 1 Chip Select N/C if not used	O CMOS – 3.3V Suspend	
SPI_MISO	A92	Data in to Module from Carrier SPI Carrier Board: Connect 15~33Ω in series to SPI flash pin 2 Serial Output N/C if not used	I CMOS – 3.3V Suspend	
SPI_MOSI	A95	Data out from Module to Carrier SPI Carrier Board: Connect 33~47 Ω in series to SPI flash pin 5 Serial Input N/C if not used	O CMOS – 3.3V Suspend	
SPI_CLK	A94	Clock from Module to Carrier SPI Carrier Board: Connect 33~47 Ω in series to SPI flash pin 6 Clock N/C if not used	O CMOS – 3.3V Suspend	

Notes:

Signal	Pin#	Description	I/O	Note
SPI_POWER	A91	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier. Carrier Board: Connect to SPI flash pin 8 VDD N/C if not used	O – 3.3V Suspend	
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device. The Carrier should only float these or pull them low, please refer to for strapping options of BIOS disable signals. Carrier Board: 1 - N/C 0 - PD 1K to GND BIOS options are shown in Table "Effect of the BIOS disable signals"	I CMOS	
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device. The Carrier should only float these or pull them low, please refer to Table X: Effect of the BIOS disable signals on page 119 below for strapping options of BIOS disable signals. Carrier Board: 1 - N/C 0 - PD 1K to GND BIOS options are shown in Table "Effect of the BIOS disable signals"	I CMOS	

The signals with the “SPI_” prefix names are used to connect directly to the regarding SPI device. SPI_CS# is the chip select signal and is usually sourced from the Module's chipset SPI0 or SPI1 signal. SPI_MISO and SPI_MOSI are the input and output signals and SPI_CLK offers the clock from the Module to the carrier's device. The SPI_POWER pin can be used to power the SPI devices and it should use less than 100mA in total. The signal is helpful to simplify the SPI schematic, because the Module's SPI power domain can be either in power state S0 or in S5.

BIOS_DIS[0:1]# signals are used to determine the boot device according to Table X: Effect of the BIOS disable signals below. BIOS_DIS0# (formerly known as BIOS_DISABLE# in COM.0 R1.0) is used to disable the on-module BIOS device and enable the LPC firmware hub. For SPI BIOS flash device usage

the signal BIOS_DIS1# should be activated to disable the on-module BIOS device and enable the BIOS flash chip on the carrier.

Table 34: Effect of the BIOS disable signals

BIOS_DIS1#	BIOS_DIS0#	Chipset SPI CS1# Destination	Chipset SPI CS0# Destination	Carrier SPI_CS#	SPI Descriptor	BIOS Entry	Ref Line
1	1	Module	Module	High	Module	SPI0/SPI1	0
1	0	Module	Module	High	Module	Carrier FWH	1
0	1	Module	Carrier	SPI0	Carrier	SPI0/SPI1	2
0	0	Carrier	Module	SPI1	Module	SPI0/SPI1	3

Notes:

2.13.2 SPI Routing Guidelines

NA

2.13.3 SPI Trace Length Guidelines

Figure 24: Topology for SPI

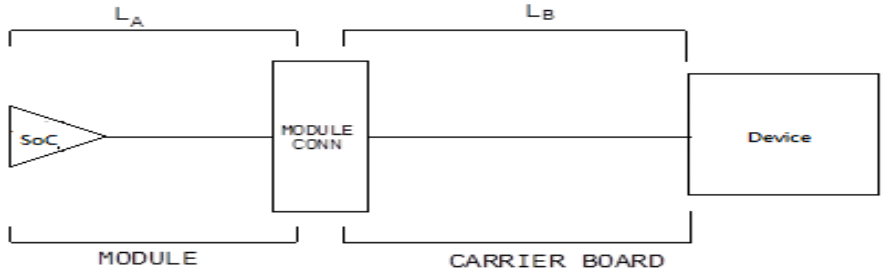


Table 35: SPI Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	SPI	
Single End	50Ω ±10%	
Nominal Trace Space within SPI Signal Group	Min. 10mils	
Spacing to Other Signal Group	Min. 15mils	
LA	Please see the SOM-7569 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	5.8”	
DATA to CLK Maximum Pin to Pin Length Mismatch	Max. 500mils	
Via Usage	Try to minimize number of vias	

Notes:

2.14 General Purpose I2C Bus Interface

The I2C (Inter-Integrated Circuit) bus is a two-wire serial bus originally defined by Philips. The bus is used for low-speed (up to 400kbps) communication between system ICs. The bus is often used to access small serial EEPROM memories and to set up IC registers. The COM Express Specification defines several I2C interfaces that are brought to the Module connector for use on the Carrier. Some of these interfaces are for very specific functions (VGA, LVDS, and DDIX), one interface is the SMBus used primarily for management and one other interface is a general purpose I2C interface. Since COM.0 Rev. 2.0 this interface should support multi-master operation. This capability will allow a Carrier to read an optional Module EEPROM before powering up the Module.

Revision 1.0 of the specification placed the I2C interface on the non-standby power domain. With this connection, the I2C interface can only be used when the Module is powered on. Since the I2C interface is used to connect to an optional Carrier EEPROM and since it is desirable to allow a Module based board controller access to the optional Carrier EEPROM before the Module is powered on, revision 2.0 of this specification changes the power domain of the I2C interface to standby-power allowing access during power down and suspend states. There is a possible leakage issue that can arise when using a R2.0 Module with a R1.0 Carrier that supports I2C devices. The R1.0 Carrier will power any I2C devices from the non-standby power rail. A R2.0 Module will pull-up the I2C clock and data lines to the standby-rail through a 2.2K resistor. The difference in the power domains on the Module and Carrier can provide a leakage path from the standby power rail to the non-standby power rail.

Vendor interoperability is given via EAPI – Embedded Application Programming Interface, which allows and easier interoperability of COM Express Modules.

2.14.1 Signal Definitions

The general purpose I2C Interface is powered from 3.3V suspend rail. The I2C_DAT is an open collector line with a pull-up resistor located on the Module. The I2C_CK has a pull-up resistor located on the Module. The Carrier should not contain pull-up resistors on the I2C_DAT and I2C_CK signals. Carrier based devices should be powered from 3.3V suspend voltage. The use of main power line for a Carrier I2C device will require a bus isolator to prevent leakage to other I2C devices on 3.3V power.

At this time, there is no allocation of I2C addresses between the Module and Carrier. Carrier designers will need to consult with Module providers for address ranges that can be used on the Carrier.

Table 36 35: General Purpose I2C Interface Signal Descriptions

Signal	Pin#	Description	I/O	Pwr Rail	Note
I2C_CK	B33	General Purpose I2C Clock output Carrier Board: 3.3VSB I2C device - Connect to SCL of I2C device. 3.3V I2C device - Connect 3.3V isolation circuit controlled by COME pin B24 PWR_OK to SCL of I2C device. 5VSB I2C device - Connect 5VSB Level Shifter to SCL of I2C device. 5V I2C device – Connect an 5V isolation circuit controlled by COME pin B24 PWR_OK to SCL of I2C device. N/C if not used	I/O OD CMOS	3.3V Suspend	
I2C_DAT	B34	General Purpose I2C data I/O line. Carrier Board: 3.3VSB I2C device - Connect to SDA of I2C device. 3.3V I2C device - Connect 3.3V isolation circuit controlled by COME pin B24 PWR_OK to SDA of I2C device 5VSB I2C device - Connect 5VSB Level Shifter to SDA of I2C device 5V I2C device - Connect an 5V isolation circuit controlled by COME pin B24 PWR_OK to SDA of I2C device N/C if not used	I/O OD CMOS	3.3V Suspend	

2.14.2 I2C Routing Guidelines

NA

2.14.3 I2C Trace Length Guidelines

Figure 25: Topology for I2C

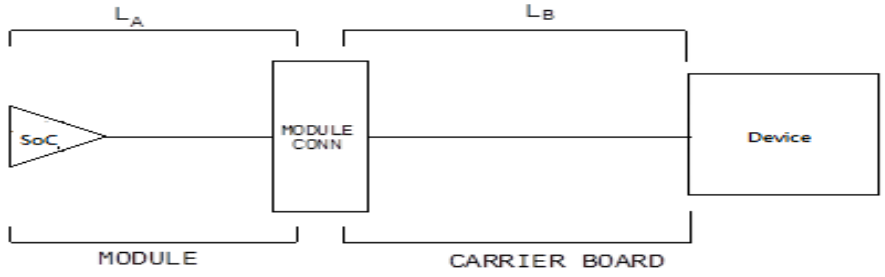


Table 37: I2C Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	I2C	
Single End	50Ω ±10%	
Nominal Trace Space within SPI Signal Group	Min. 10mils	
Spacing to Other Signal Group	Min. 15mils	
LA	Please see the SOM-7569 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	ASAP	
Length Mismatch	NA	
Via Usage	Try to minimize number of vias	

Notes:

2.14.4 Connectivity Considerations

The maximum amount of capacitance allowed on the Carrier General Purpose I2C bus lines (I2C_DAT, I2C_CK) is specified by Advantech's Module. The Carrier designer is responsible for ensuring that the maximum amount of capacitance is not exceeded and the rise/fall times of the signals meet the I2C bus specification. As a general guideline, an IC input has 8pF of capacitance, and a PCB trace has 3.8pF per inch of trace length.

2.15 System Management Bus (SMBus)

The SMBus is primarily used as an interface to manage peripherals such as serial presence detect (SPD) on RAM, thermal sensors, PCI/PCIe devices, smart battery, etc. The devices that can connect to the SMBus can be located on the Module and Carrier. Designers need to take note of several implementation issues to ensure reliable SMBus interface operation. The SMBus is similar to I2C. I2C devices have the potential to lock up the data line while sending information and require a power cycle to clear the fault condition. SMBus devices contain a timeout to monitor for and correct this condition. Designers are urged to use SMBus devices when possible over standard I2C devices. COM Express Modules are required to power SMBus devices from Early Power in order to have control during system states S0-S5. The devices on the Carrier Board using the SMBus are normally powered by the 3.3V main power. To avoid current leakage between the main power of the Carrier Board and the Suspend power of the Module, the SMBus on the Carrier Board must be separated by a bus switch from the SMBus of the Module. However, if the Carrier Board also uses Suspend powered SMBus devices that are designed to operate during system states S3-S5, then these devices must be connected to the Suspend powered side of the SMBus, i. e. between the COM Express Module and the bus switch. Since the SMBus is used by the Module and Carrier, care must be taken to ensure that Carrier based devices do not overlap the address space of Module based devices. Typical Module located SMBus devices and their addresses include memory SPD (serial presence detect 1010 000x, 1010 001x), programmable clock synthesizes (1101 001x), clock buffers (1101 110x), thermal sensors (1001 000x), and management controllers (vendor defined address). Contact Advantech for information on the SMBus addresses used.

2.15.1 SMB Signal Definitions

Table 38: SMB Signal Definitions

Signal	Pin#	Description	I/O	Pwr Rail	Note
SMB_CK	B13	System Management Bus bidirectional clock line Carrier Board: 3.3VSB SMBus device - Connect to SMBCLK of SMBus device. 3.3V SMBus device - Connect 3.3V isolation circuit controlled by COME pin B24 PWR_OK to SMBCLK of SMBus device. 5VSB SMBus device - Connect 5V Level Shifter to SMBCLK of SMBus device. 5V SMBus device - Connect 5V isolation circuit controlled by COME pin B24 PWR_OK to SMBCLK of SMBus device N/C if not used.	I/O OD CMOS	3.3V Suspend rail	
SMB_DAT	B14	System Management bidirectional data line. Carrier Board: 3.3VSB SMBus device - Connect to SMBDAT of SMBus device. 3.3V SMBus device - Connect 3.3V isolation circuit controlled by COME pin B24 PWR_OK to SMBDAT of SMBus device. 5VSB SMBus device - Connect 5V Level Shifter to SMBDAT of SMBus device. 5V SMBus device - Connect 5V isolation circuit controlled by COME pin B24 PWR_OK to SMBDAT of SMBus device N/C if not used.	I/O OD CMOS	3.3V Suspend rail	
SMB_ALERT#	B15	System Management Bus Alert Carrier Board: Connect to SMBALERT# of SMBus device. N/C if not used.	I CMOS	3.3V Suspend Rail	

Note:

2.15.2 SMB Routing Guidelines

The SMBus should be connected to all or none of the PCIe/PCI devices and slots. A general recommendation is to not connect these devices to the SMBus.

The maximum load of SMBus lines is limited to 3 external devices. Please contact Advantech if more devices are required.

Do not connect Non-Suspend powered devices to the SMBus unless a bus switch is used to prevent back feeding of voltage from the Suspend rail to other supplies.

Contact Advantech for a list of SMBus addresses used on the Module. Do not use the same address for Carrier located devices.

2.15.3 SMB Trace Length Guidelines

Figure 26: Topology for SMB

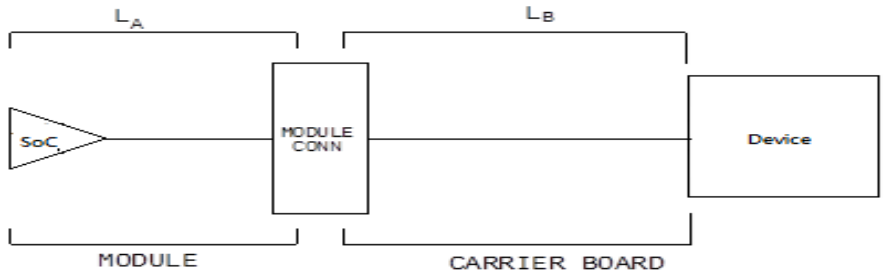


Table 39: SMB Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	SMB	
Single End	50Ω ±10%	
Nominal Trace Space within SPI Signal Group	Min. 10mils	
Spacing to Other Signal Group	Min. 15mils	
LA	Please see the SOM-7569 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	ASAP	
Length Mismatch	NA	
Via Usage	Try to minimize number of vias	

Notes:

2.16 General Purpose Serial Interface

Advantech provides two serial ports on Type 10 and Type 6 COM Express Modules.

2.16.1 Serial interface Signal Definitions

Table 40: Serial interface Signal Definitions

Signal	Pin#	Description	I/O	Note
SER0_TX	A98	Transmit Line for Serial Port 0 Carrier Board: SER0_TX need pull down 4.7K ohm, refer to Figure 29. connect to Device - TXD COM DB-9 port - TxIN of Serial Transceiver and TxOUT to DB-9 pin 3 TXD N/C if not used.	O CMOS	
SER0_RX	A99	Receive Line for Serial Port 0 Carrier Board: Connect to Device - RXD COM DB-9 port - TxOUT of Serial Transceiver and TxIN to DB-9 pin 2 RXD N/C if not used	I CMOS	
SER1_TX	A101	Transmit Line for Serial Port 1 Carrier Board: SER1_TX need pull down 4.7K ohm, refer to Figure 29. connect to Device - TXD COM DB-9 port - TxIN of Serial Transceiver and TxOUT to DB-9 pin 3 TXD N/C if not used.	O CMOS	
SER1_RX	A102	Receive Line for Serial Port 1 Carrier Board: Connect to Device - RXD COM DB-9 port - TxOUT of Serial Transceiver and TxIN to DB-9 pin 2 RXD N/C if not used	I CMOS	

Note:

2.16.2 Serial interface Routing Guidelines

NA

2.16.3 Serial interface Trace Length Guidelines

Figure 27: Topology for Serial interface

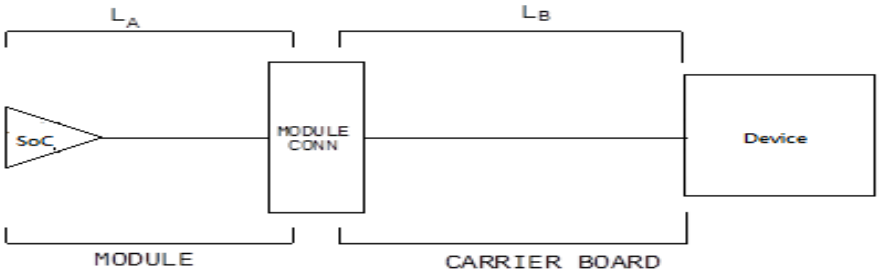


Table 41: Serial interface Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	Serial interface	
Single End	50Ω ±10%	
Nominal Trace Space within SPI Signal Group	Min. 10mils	
Spacing to Other Signal Group	Min. 15mils	
LA	ASAP	
LB	Carrier Board Length	
Max length of LA+LB	NA	
Length Mismatch	NA	
Via Usage	Try to minimize number of vias	

Notes:

2.17 CAN Interface

CAN bus is a vehicle bus standard designed to allow controllers and devices to communicate with each other without a host computer. CAN bus is a message-based protocol, designed specifically for automotive applications but now also used in other areas such as industrial automation and medical equipment.

Development of CAN bus started originally in 1983. The protocol was officially released in 1986 at the Society of Automotive Engineers (SAE) congress in Detroit, Michigan. The first CAN controller chips, produced by Intel and Philips, came on the market in 1987. In 1991 the CAN 2.0 specification was published.

Since 2008 CAN bus has been mandatory in any US vehicle in the OBD-II car diagnostic port. It is also used extensively in industrial automation.

2.17.1 CAN interface Signal Definitions

Table 42: CAN interface Signal Definitions

Signal	Pin#	Description	I/O	Note
CAN_TX	A101	Transmit Line for CAN Carrier Board: CAN_TX need pull down 4.7K ohm, refer to Figure 29. Check your CAN transceiver application notes.	O CMOS	1
CAN_RX	A102	Receive Line for CAN Carrier Board: Check your CAN transceiver application notes.	I CMOS	1

Note:

1. SOM-7569 default is serial interface. BOM option with CAN interface.

2.17.2 CAN interface Routing Guidelines

It should be routed as a differential pair signal with 120 Ohm differential impedance. The end points of CAN bus should be terminated with 120 Ohms or with 60 Ohms from the CAN_H line and 60 Ohms from the CAN_L line to the CAN Bus reference voltage. Check your CAN transceiver application notes for further details on termination.

2.17.3 CAN interface Trace Length Guidelines

Figure 28: Topology for CAN interface

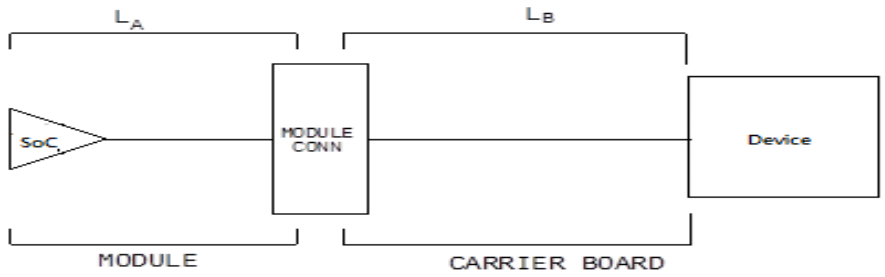


Table 43: CAN interface Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	CAN interface	1
Single End	NA	
Nominal Trace Space within SPI Signal Group	Min. 10mils	
Spacing to Other Signal Group	Min. 15mils	
LA	ASAP	
LB	Carrier Board Length	
Max length of LA+LB	NA	
Length Mismatch	NA	
Via Usage	Try to minimize number of vias	

Notes:

1. SOM-7569 default is serial interface. BOM option with CAN interface.

2.18 Miscellaneous Signals

2.18.1 Miscellaneous Signals

Table 44: Miscellaneous Signal Definitions

Signal	Pin#	Description	I/O	Note
TYPE10#	A97	Indicates to the Carrier Board that a Type 10 Module is installed. Indicates to the Carrier Board, that a Rev 1.0/2.0 Module is installed. TYPE10# NC Pin-out R2.0 PD Pin-out Type 10 pull down to ground with 47k 12V Pin-out R1.0		
SPKR	B32	Output used to control an external FET or a logic gate to drive an external PC speaker. Carrier Board: Connect to Speaker circuit. N/C if not used	O 3.3V CMOS	
BIOS_DISABLE0#	A34	Selection straps to determine the BIOS boot device. The Carrier should only float these or pull them low.	I 3.3V CMOS	See Section 2.13 'SPI – Serial Peripheral Interface Bus'
BIOS_DISABLE1#	B88	Selection straps to determine the BIOS boot device. The Carrier should only float these or pull them low.	I 3.3V CMOS	See Section 2.13 'SPI – Serial Peripheral Interface Bus'
WDT	B27	Output indicating that a watchdog time-out event has occurred. Carrier Board: Connect to Watchdog trigger input. N/C if not used	O 3.3V CMOS	

Signal	Pin#	Description	I/O	Note
LID#	A103	LID switch. Low active signal used by the ACPI operating system for a LID switch. Carrier Board: R1.0/R2.x Module both - Connect protection scheme referred to Figure 29 to LID button. R2.x Module only - Connect to LID button. N/C if not used.	I 3.3V CMOS OD	
SLEEP#	B103	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again. Carrier Board: R1.0/R2.x Module both - Connect protection scheme referred to Figure 29 to Sleep button. R2.x Module only - Connect to Sleep button. N/C if not used	I 3.3V CMOS OD	
FAN_PWMOUT	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM. Carrier Board: R1.0/R2.x Module both - Connect protection scheme referred to Figure 29 to FAN connector pin 2 PWMOUT via Smart FAN circuit R2.x Module only - PD 4.7KΩ to GND and connects to FAN connector pin 2 PWMOUT via Smart FAN circuit N/C if not used	O 3.3V CMOS OD	

Signal	Pin#	Description	I/O	Note
FAN_TACHIN	B102	Fan tachometer input for a fan with a two pulse output. Carrier Board: R1.0/R2.x Module both - Connect protection scheme referred to Figure 29 to FAN connector pin 3 TACHIN via Smart FAN circuit R2.x Module only - Connect to FAN connector pin 3 TACHIN via Smart FAN circuit N/C if not used	I 3.3V CMOS OD	
TPM_PP	A96	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM. Carrier Board: Physical Absence - N/C Physical Presence - PU 1KΩ to 3.3V N/C if not used	I 3.3V CMOS	
GPO0 / SDIO_CLK GPO1 / SDIO_CMD GPO2 / SDIO_WP GPO3 / SDIO_CD#	A93 B54 B57 B63	General Purpose Outputs for system specific usage. Internal pull up 75Kohm on the module. Carrier Board: Connect to GPO[3..0] N/C if not used	O 3.3V CMOS	1
GPI0 / SDIO_DAT0 GPI1 / SDIO_DAT1 GPI2 / SDIO_DAT2 GPI3 / SDIO_DAT3	A54 A63 A67 A85	General Purpose Input for system specific usage. Internal pull up 75Kohm on the module. Carrier Board: Connect to GPI[3..0] N/C if not used	I 3.3V CMOS	1
VCC_RTC	A47	Real-time clock circuit power input. Nominally +3.0V		

Note:

1. **SDIO Interface Multiplexed with GPIOs**

SD Card support was added in COM.0 Rev. 2.0 as an alternative use for the GPIO pins.

SOM-7569 don’t support SDIO by default.

Table 45: Signal Definition SDIO

Signal	Pin#	Description	I/O	Notes
SDIO_CD#	B63	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present. Carrier Board: Connect to CD# of SDIO/MMC device or card N/C if not used	I 3.3V CMOS	1
SDIO_CLK	A93	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48 MHz Carrier Board: Connect 10Ω near to SDIO connector Connect to CLK of SDIO/MMC device or card N/C if not used	O 3.3V CMOS	1
SDIO_CMD	B54	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode. Carrier Board: Connect 10Ω near to SDIO connector Connect to CMD of SDIO/MMC device or card N/C if not used	O 3.3V CMOS	1
SDIO_WP	B57	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards. Carrier Board: Connect to WP of SDIO/MMC device or card N/C if not used	I 3.3V CMOS	1
SDIO_DAT0 SDIO_DAT1 SDIO_DAT2 SDIO_DAT3	A54 A63 A67 A85	SDIO Data lines. These signals operate in push-pull mode. Carrier Board: Connect 10Ω near to SDIO connector Connect to DATA0-3 of SDIO/MMC device or card N/C if not used	I/O 3.3V CMOS	1

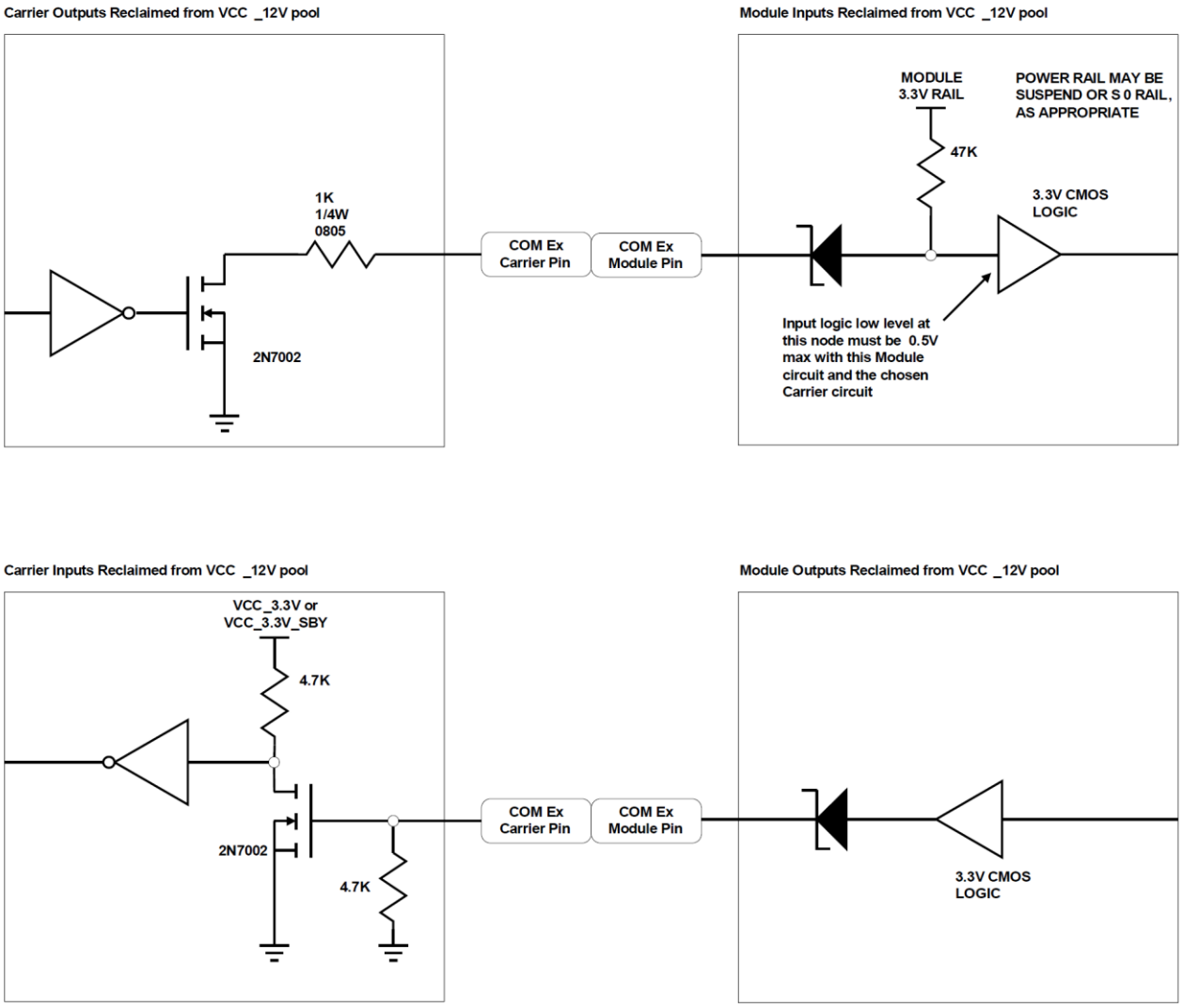
Note:

1. SOM-7569 don't support SDIO by default.

2.18.1.1 Logic Level Signals on Pins Reclaimed from VCC_12

Carrier Board logic level inputs and outputs that are implemented on pins reclaimed from the VCC_12V pool shall be protected against protracted accidental exposure to 12V. The protection scheme shown in the left side of the Figure 29 below may be used. Any scheme that is used shall be able to pull the reclaimed Module input low enough such that Module CMOS input logic sees a maximum voltage of 0.5V for a logic low, as indicated in the figure.

Figure 29: Protecting Logic Level Signals on Pins Reclaimed from VCC_12V



2.18.2 Power Management Signals

Table 46: Power Management Signal Definitions

Signal	Pin#	Description	I/O	Note
PWRBTN#	B12	Power button low active signal used to wake up the system from S5 state (soft off). This signal is triggered on the falling edge. Module has integrated PU resistor 10K ohm to 3.3V suspend power and has an internal 50 ms de-bounce on the input. Carrier Board: ATX - Connect to Power Button or SIO Power Button output pin (Active low) AT - N/C N/C if not used	I 3.3V Suspend CMOS	
SYS_RESET#	B49	Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used. Carrier Board: Connect to Reset button N/C if not used	I 3.3V Suspend CMOS	
CB_RESET#	B50	Reset output signal from Module to Carrier Board. This signal may be driven low by the Module to reset external components located on the Carrier Board. Carrier Board: Connect to reset pin of devices except PCI slots or devices. N/C if not used.	O 3.3V Suspend CMOS	
PWR_OK	B24	Power OK status signal generated by the ATX power supply to notify the Module that the DC operating voltages are within the ranges required for proper operation. Carrier Board: Connect to power good pin of main power supply ATX - PW-OK pin 8 of ATX power connector connects 3.3V level shifter to COME PWR_OK. AT - PG pin P8.1 of AT power connector connects 3.3V level shifter to COME PWR_OK. Other - PWROK of 12V power generator circuit connects 3.3V level shifter to COME PWR_OK. N/C is not allowed, if the system is ATX mode. N/C if not used.	I 3.3V CMOS	

Signal	Pin#	Description	I/O	Note
SUS_STAT#	B18	Suspend status signal to indicate that the system will be entering a low power state soon. It can be used by other peripherals on the Carrier Board as an indication that they should go into power-down mode. Carrier Board: Connect to LPCPD# of LPC device. N/C if not used.	O 3.3V Suspend CMOS	
SUS_S3#	A15	S3 Sleep control signal indicating that the system resides in S3 state (Suspend to RAM). This signal can be used to control the ATX power supply via the *'PS_ON#'* signal. Carrier Board: Connect to SLP_S3# (Suspend To RAM) of LPC device or SIO. N/C if not used.	O 3.3V Suspend CMOS	
SUS_S4#	A18	S4 Sleep control signal indicating that the system resides in S4 state (Suspend to Disk). Carrier Board: Connect to SLP_S4# (Suspend To Disk) of LPC device or SIO. N/C if not used.	O 3.3V Suspend CMOS	
SUS_S5#	A24	S5 Sleep Control signal indicating that the system resides in S5 State (Soft Off). Carrier Board: Connect to SLP_S5# (Soft Off) of LPC device or SIO. N/C if not used.	O 3.3V Suspend CMOS	
WAKE1#	B67	General purpose wake-up signal. Carrier Board: Connect to PME# of SIO N/C if not use	I 3.3V Suspend CMOS	
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low. It also can be used to signal some other external power management event. Carrier Board: Connect to BATLOW# of Smart Battery. N/C if not used.	I 3.3V Suspend CMOS	

Note:

2.18.3 Thermal Interface

Table 47: Thermal Management Signal Definitions

Signal	Pin#	Description	I/O	Note
THRM#	B35	Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling. Carrier Board: Connect to THRM# output of Hardware Monitor. N/C if not used.	I 3.3V CMOS	1
THRMTRIP#	A35	Thermal Trip indicates an overheating condition of the processor. If *'THRMTRIP#'* goes active the system immediately transitions to the S5 State (Soft Off). Carrier Board: Connect to THERMTRIP# input of devices. N/C if not used.	O 3.3V CMOS	

Note:

1. Carrier board don't need to pull down.

2.18.4 Miscellaneous Signals Routing Guidelines

NA

2.18.5 SDIO Signals Trace Length Guidelines

Figure 30: Topology for SDIO

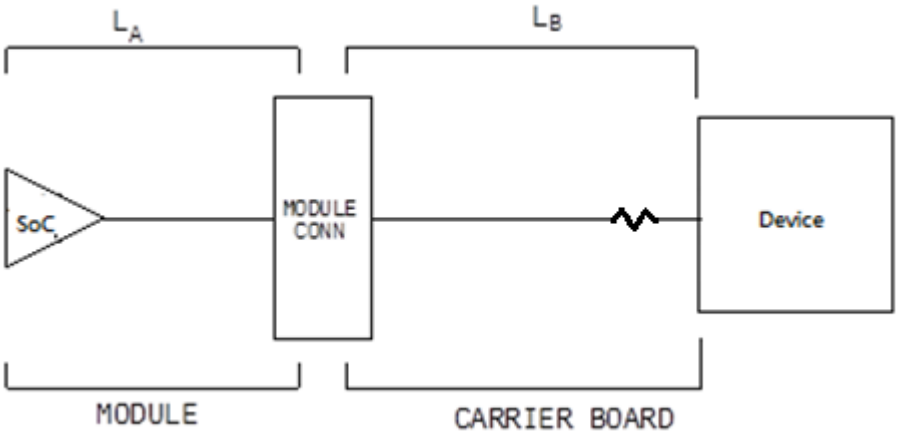


Table 48: SDIO Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	SDIO	
Single End	50Ω ±10%	
DATA to CLK Maximum Pin to Pin Length Mismatch	200 mils	
Main Route segment for CMD/Data/CD#	Minimum Trace Spacing Between Other SD Card and Interface Signals 15 mils	
Main Route segment for CLK)	Minimum Trace Spacing Between Other SD Card and Interface Signals 15mils	
Spacing to Other Signal Group	Min. 15mils	
LA	Please see the SOM-7569 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	7”	
Length matching	Data/CMD to Clock must be matched within 200mils	
Reference Plane	Continuous ground only	
Via Usage	Max 2 vias	

Notes:

1. SDIO CLK/DATAs/CMD connects 10Ω near to SDIO connector within 100mils.

2.19 Reserved Pins.

RSVD pins are reserved for future use and should be no connect. But Advantech maybe use for another function, please see the 2.19.1 description.

2.19.1 Reserved Pins Definitions

Table 49: RSVD Definitions

Signal	Pin#	Description	I/O	Note
RSVD	A52	Reserved pin.		
RSVD	A53	Reserved pin.		
RSVD	A55	Reserved pin.		
RSVD	A56	Reserved pin.		
RSVD	A86	Reserved pin.		
RSVD	B52	Reserved pin.		
RSVD	B53	Reserved pin.		
RSVD	B55	Reserved pin.		
RSVD	B56	Reserved pin.		

Note:

3 Power

3.1 General Power requirements

COM Express calls for the Module to be powered by a single 12V power rail, with a +/-5% tolerance. The Mini format Modules are specified in COM.0 Rev. 2.1 to support a power input range of 4.75V to 20.0V. Advantech offer a wide range input even on Compact and Basic Modules. COM Express Modules may consume significant amounts of power – 25 to 50W is common, and higher levels are allowed by the standard. Close attention must be paid by the Carrier Board designer to ensure adequate power delivery. Details are given in the sections below.

If Suspend functions such as Suspend-to-RAM, Suspend-to-disk, wake on power button press, wake on USB activity, etc. are to be supported, then a 5V Suspend power source must also be provided to the Module. If Suspend functions are not used, the Module VCC_5V_SBY pins should be left open. On some Modules, there may be a slight power efficiency advantage to connecting the Module VCC_5V_SBY rail to VCC_5V rather than leaving the Module pin open.

Please contact Advantech for further details. Carrier Boards typically require other power rails such as 5V, 3.3V, 3.3V Suspend, etc. These may be derived on the Carrier Board from the 12V and 5V Suspend rails.

3.2 VCC5_SBY Routing

The +5V Suspend power rail, if used, should be sized to handle 2A. Most, but not all, Modules will use considerably less than 2A for this power rail. Modules with multiple Ethernet channels and wake-on-LAN capability will use more current. The COM Express Specification allows up to 2A on this rail. Advantech recommends design 2A for VCC5_SBY.

3.3 ATX and AT Power Sequencing Diagrams

A sequence diagram for an ATX style boot from a soft-off state (S5), initiated by a power button press, is shown in Figure 31 below.

A sequence diagram for an AT style boot from the mechanical off state (G3) is shown in Figure 32 below .

In both cases, the VCC_12V, VCC_5V and VCC_3V3 power lines should rise together in a monotonic ramp with a positive slope only, and their rise time should be limited. Please refer to the ATX specification for more details.

Figure 31: ATX Style Power Up Boot – Controlled by Power Button

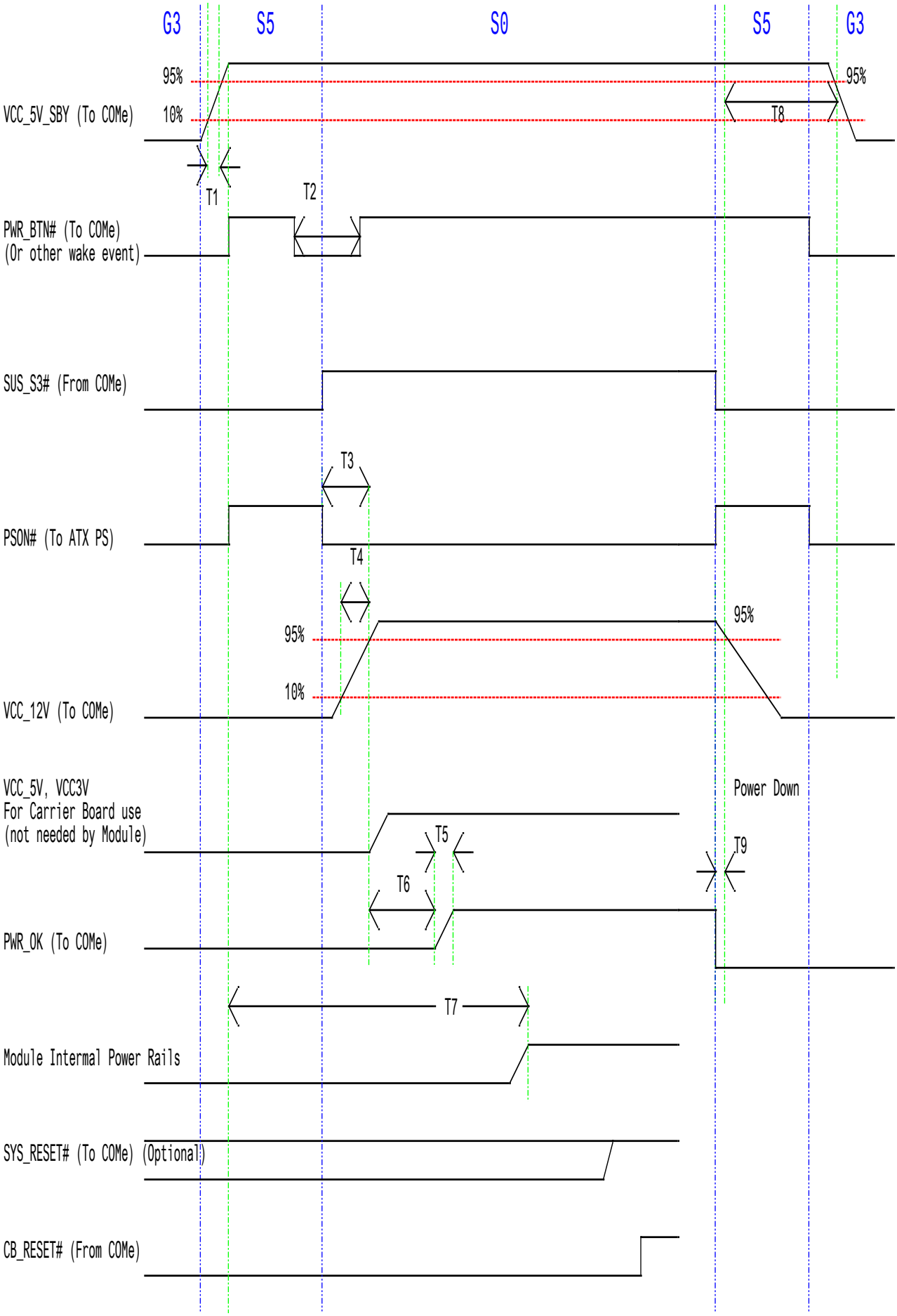


Figure 32: AT Style Power Up Boot

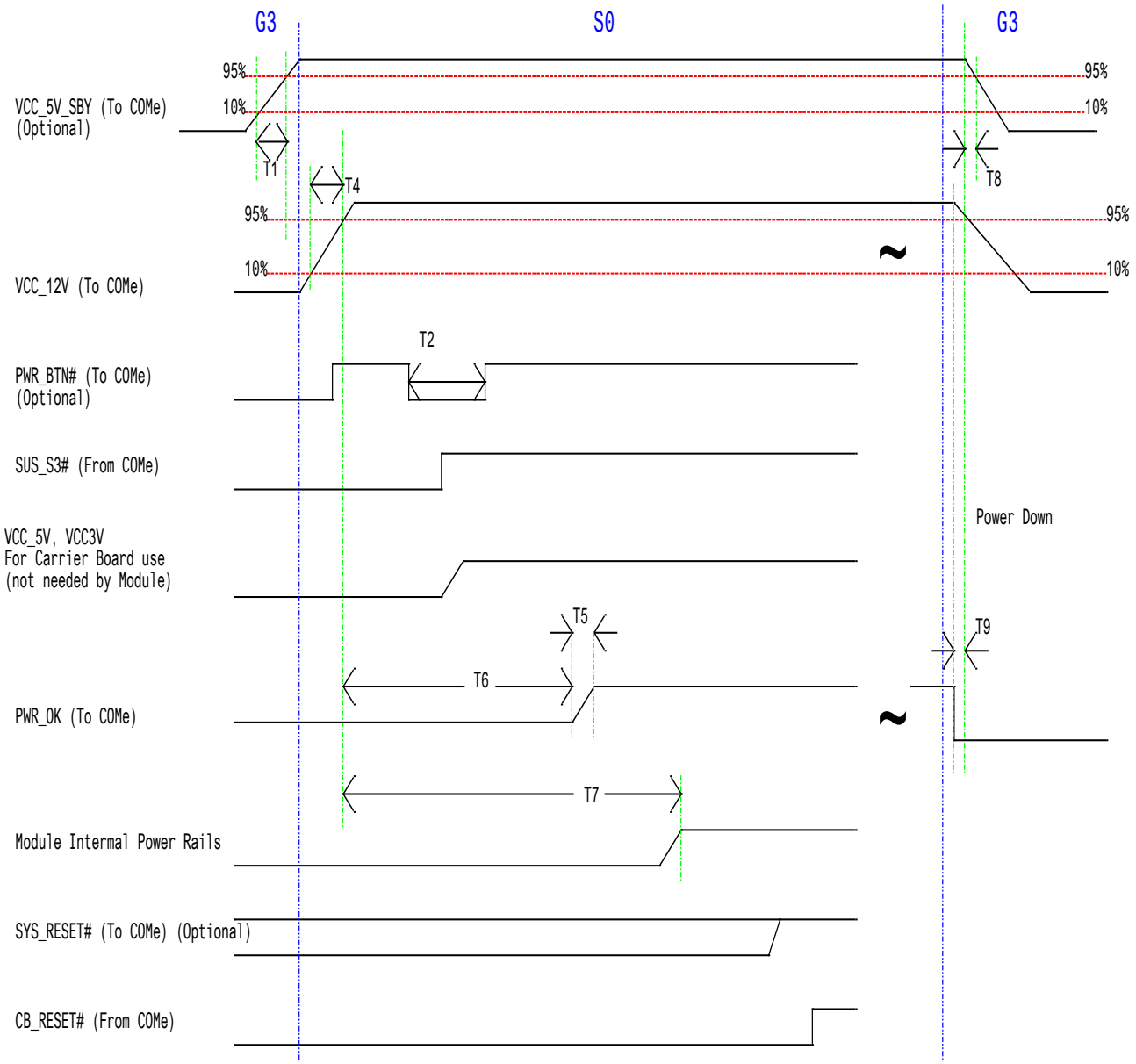


Table 50: Power Management Timings

Sym	Description	Min	Max
T1	VCC_5V_SBY rise time from 10% to 95%	0.1ms	20ms
T2	Power Button	50ms	
T3	The power-on time is defined as the time from when PS_ON# is pulled low to when the VCC_12V, VCC_5V and VCC_3V output 95%.		500ms
T4	VCC_12V rise time from 10% to 95%	0.1ms	20ms
T5	PWR_OK rise time		10ms
T6	VCC_12V rise 95% to PWROK rise	0ms	
T7	See Note 1	1ms	
T8	VCC_12V fall 95% to VCC_5V_SBY fall 95%	0ms	
T9	PWR_OK fall to VCC_12V fall 95%.	1ms	

Note:

1. There is a period of time (T6 in Figure 31 and Figure 32 above) during which the Carrier Board circuits have power but the COM Express Module main internal power rails are not up. This is because almost all COM Express internal rails are derived from the external VCC_12V and there is a non-zero start-up time for the Module internal power supplies.

   Carrier Board circuits should not drive any COM Express lines during the T6 interval except for those identified in the COM Express Specification as being powered from a Suspend power rail. Almost all such signals are active low. Such signals, if used, should be driven low by open drain Carrier Board circuits to assert them. Pull-ups, if present, should be high value (10K to 100K) and tied to VCC_5V_SBY.

   The line PWR_OK may be used during the T6 interval to hold off a COM Express Module boot. Sometimes this is done, for example, to allow a Carrier Board device such as an FPGA to be configured before the Module boots.

   The deployment of Carrier Board pull-ups on COM Express signals should be kept to a minimum in order to avoid back-driving the COM Express signal pins during this interval.
   Carrier Board pull-ups on COM Express signal pins are generally not necessary – most signals are pulled up if necessary on the Module.

3.4 Input Power - Rise Time

The input voltages to the COM Express Module VCC_12V, wide input (Mini) and VCC_5V_SBY if used shall rise from ≤10% of nominal to within the regulation ranges within 0.1 ms to 20 ms (0.1 ms ≤ T1/T4 ≤ 20 ms). There must be a smooth and continuous ramp of each DC output voltage from 10% to 95% of its final set point within the regulation band. The smooth turn-on requires that, during the 10% to 95% portion of the rise time, the slope of the turn-on waveform must be positive and have a value of between 0 V/ms and [Vout, nominal / 0.1] V/ms. Also, for any 5ms segment of the 10% to 95% rise time waveform, a straight line drawn between the end points of the waveform segment must have a slope ≥ [Vout, nominal / 20] V/ms.

3.5 Design Considerations for Carrier Boards containing FPGAs/CPLDs

Very often, the Carrier Board will contain custom FPGA or other programmable devices which require the loading of program code before they are usable. The Carrier Board designer needs to take the necessary precautions to ensure that his Carrier Board logic is up and running before the Module starts. Conflicts can occur if the Module is powered on and allowed to run before devices on the Carrier Board are fully programmed and initialized. A typical example is an FPGA which includes a PCIe device. Such devices must be initialized and ready before the chipset on the Module performs link training and before the BIOS code performs enumeration of PCI devices. The Module should therefore be prevented from starting before Carrier Board devices are ready.

One method to achieve this is to delay assertion of the PWR_OK# signal to the Module until the Carrier Board initialization process has completed. Note that during the phase when the Carrier Board is powered and the Module is not powered there is potential for back drive voltages from the carrier to the Module.

Another possibility is to use the SYS_RESET# signal to delay Module start-up. However, depending on the Module implementation and the chipset used, SYS_RESET# may only be a falling edge triggered signal and not a low active signal as was originally intended. In that case, asserting SYS_RESET# may not hold the Module in the reset state. Also, PCIe link training will occur regardless of the reset signal state for some chipsets.

Please refer to the COM.0 R2.1 specification (Power and System Management section) for more details and check the Module provider’s documentation for their implementations of these signals.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 51: Absolute Maximum Ratings

SOM-7569		MIN	MAX	UNIT
Power	VIN	4.75 (5-5%)	20 (19+5%)	V
	VSB	4.75 (5-5%)	5.25 (5+5%)	V
	RTC Battery	2.0	3.3	V

4.2 DC Characteristics

Table 52: Input Power Consumption of 12V / 4.75V / 20V

Intel(R) Atom(TM) Processor E3950 @1.6GHz ,MICRON_MT41K1G8 SN-107 IT:A 8GB					
Power Plane	Maximum Power Consumption				
Symbol	S0		S3	S5	G3
+VIN (+12V)	TAT CPU+GPU100%	22.679W			
	Idle	7.545W			
+VIN (+4.75V)	TAT CPU+GPU100%	24.742W			
	Idle	6.043W			
+VIN (+20V)	TAT CPU+GPU100%	23.204W			
	Idle	6.744W			
+V5SB_CB	0.050W		0.669W	0.567W	
RTC Battery				1.57uA	6.22uA

4.3 Inrush Current

Table 53: Inrush Current

Power Plane	Maximum	
Symbol	G3 to S5	S5 to S0
+V5SB_CB	493.69mA	
+VIN (+12V)		299.92mA
+VIN (+4.75V)		417.97mA
+VIN (+20V)		289.29mA