SODIMM DDR5 5600 24GB Datasheet

(SQR-SD5N24G5K6M)

CONTENTS

Revision History

Rev	Date	Modification
0.0	1ST Jul., 2023	Official release

1. Description

DDR5 SODIMM							
Part Number	Density	Data rate	DIMM Organization	Number of DRAM	Number of rank	side	ECC
SQR-SD5N24G5K6M (Micron 3Gx8 B-die)	24GB	5600 MT/s	3Gx64	8	1	1	N

2. Features

- Key Parameter

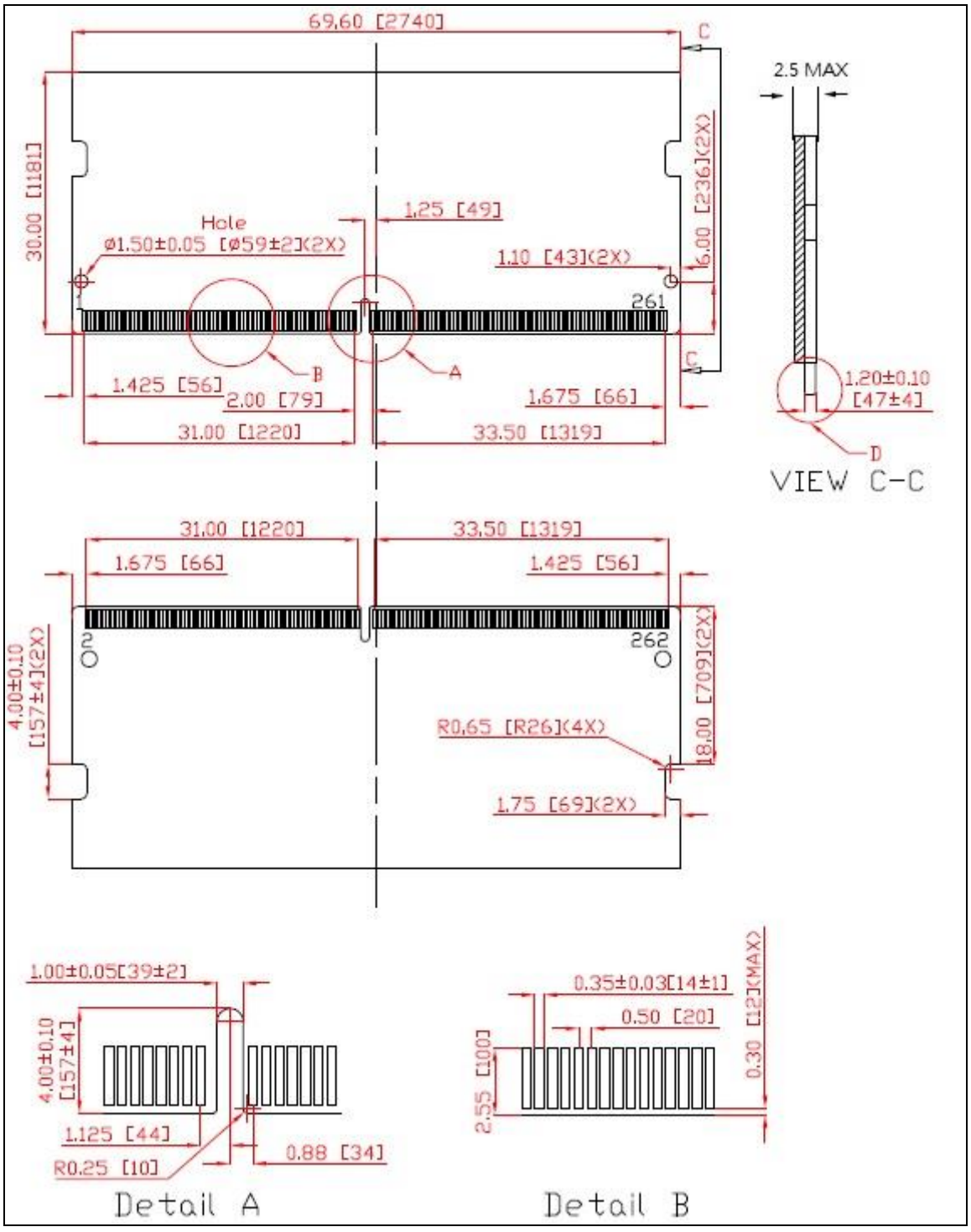
Data transfer Rate	tCK (ns)	tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)
5600 MT/s	0.357	16.00	16.00	32	48.00

- tRFC parameter by Density

Parameter	8Gb	16Gb	24Gb	32Gb	Unit
tRFC1,min	195	295	410	410	ns
tRFC2,min	130	160	220	220	ns
tRFCsb,min	115	130	190	190	ns

- JEDEC Standard 262-pin Small Outline Dual In-Line Memory Module
- Cl-tRCD-tRP: 46-45-45
- VDD=VDDQ= 1.1V (1.067V ~ 1.166V)
- VPP=1.8V (1.746V ~ 1.908V)
- VDDSPD= 1.8V
- On-die, internal, adjustable VREF generation for DQ,CA,CS
- 16n-bit prefetch
- Two independent I/O sub channels
- Programmable /CAS Latency: 22,26,28,30,32,36,40,42,46,50
- Operating temperature Tcase: 0-95°C
  - ◆ tREFI 3.9us for 0°C ≤Tcase < 85°C
  - ◆ tREFI 1.95us for 85°C < Tcase ≤ 95°C
- Fly-by topology
- I3C/I2C support
- Terminated control and C/A bus
- SPD EEPROM Hub and Integrated Thermal Sensor
- Halogen-free

3. Dimension



Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of ±0.15 (6), unless otherwise specified.

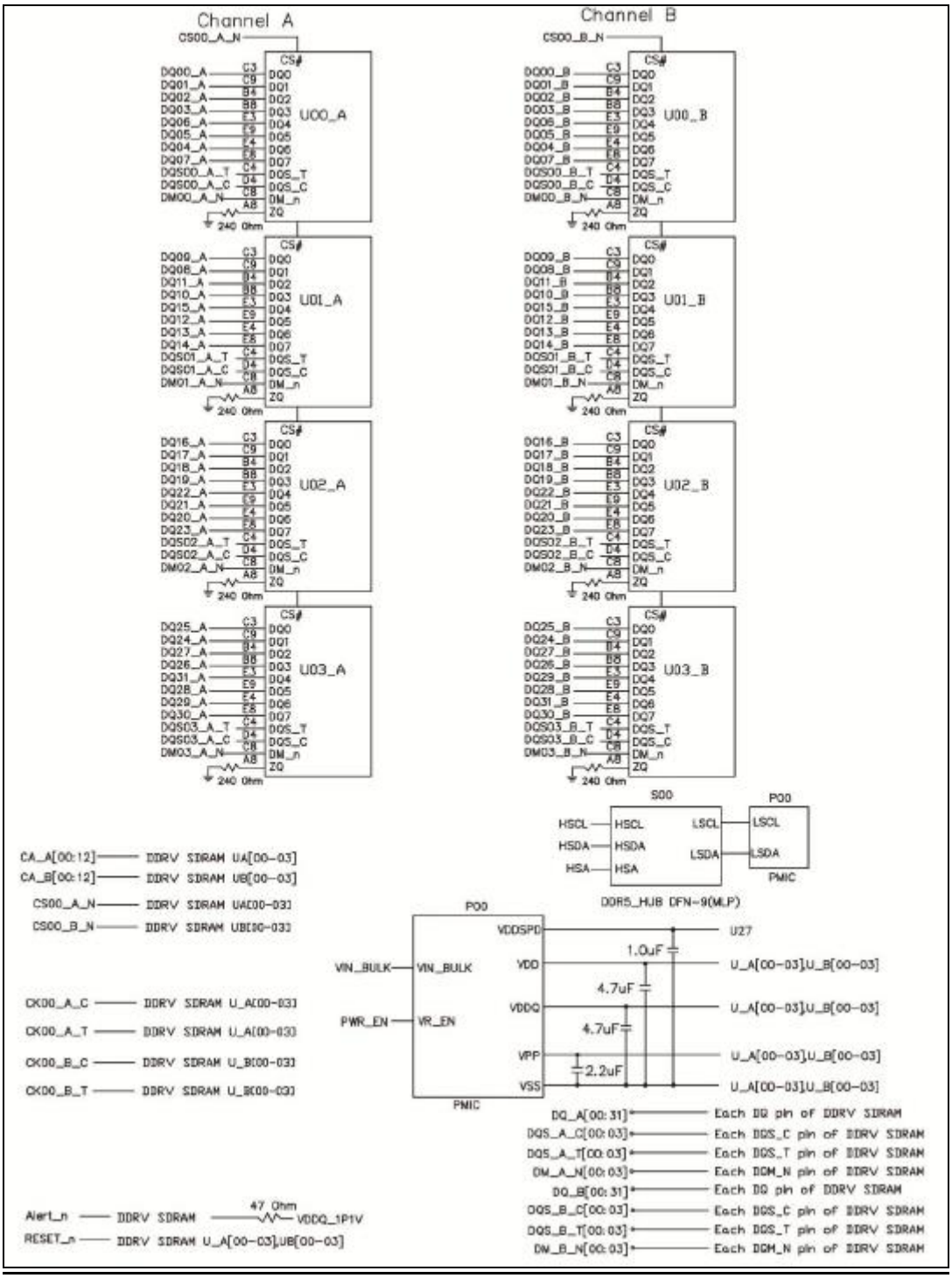
4. Pin Descriptions

Symbol	Type	I/O Level	Description	Symbol	Type	I/O Level	Description
CK_t, CK_c	Input	VDDQ	Clock	DQ[31:0]_A DQ[31:0]_B	Input/ Output	VDDQ	Data Input/Output
CA[12:0]_A CA[12:0]_B	Input	VDDQ	Command/Address Inputs	CB[3:0]_A CB[3:0]_B	Input/ Output	VDDQ	ECC Check Bits Input/Output
CS[1:0]_A CS[1:0]_B	Input	VDDQ	Chip Select	DQS[4:0]_A_t DQS[4:0]_B_t	Input/ Output	VDDQ	Data Strobe
ALERT_n	Output	VDDQ	Alert	DQS[4:0]_A_c DQS[4:0]_B_c	Input/ Output	VDDQ	Data Strobe
RESET_n	CMOS Input	VDDQ	Active Low Asynchronous Reset	DM[3:0]_A_n DM[3:0]_B_n	Input	VDDQ	Input Data Mask
PWR_GOOD	Input/ Output	VDDQ	Power Good Indicator	VIN_BULK	Supply		External Power Supply
HSCL	Input	VOUT	Host Sideband Bus Clock	PWR_EN	Input		PMIC Enable
HSDA	Input/ Output	VOUT	Host Sideband Bus Data	VSS	Supply		Ground
HSA	Input	GND	Host Sideband Bus Device ID	RFU			Reserved for future use

5. Pin Assignments

262-Pin DDR5 SODIMM Front								262-Pin DDR5 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VIN_BULK	67	Vss	133	CK0_A_c	199	DQ8_B	2	HAS	68	DQ21_A	134	CK1_A_c	200	Vss
3	VIN_BULK	69	DQ22_A	135	Vss	201	Vss	4	HSCL	70	Vss	136	Vss	202	DQ9_B
5	RFU	71	Vss	137	CK0_B_t	203	DQ10_B	6	HSDA	72	DQ23_A	138	CK1_B_t	204	Vss
7	PWR_GOOD	73	DQ24_A	139	CK0_B_c	205	Vss	8	PWR_EN	74	Vss	140	CK1_B_c	206	DQ11_B
9	Vss	75	Vss	141	Vss	207	DQS1_B_c	10	Vss	76	DQ25_A	142	Vss	208	Vss
11	DQ0_A	77	DQ26_A	143	RFU	209	DQS1_B_t	12	DQ1_A	78	Vss	144	CA12_B	210	DM1_B_n
13	Vss	79	Vss	145	CA11_B	211	Vss	14	Vss	80	DQ27_A	146	CA10_B	212	Vss
15	DQ2_A	81	DQS3_A_c	147	Vss	213	DQ12_B	16	DQ3_A	82	Vss	148	Vss	214	DQ13_B
17	Vss	83	DQS3_A_t	149	CA9_B	215	Vss	18	Vss	84	DM3_A_n	150	CA8_B	216	Vss
19	DM0_A_n	85	Vss	151	CA7_B	217	DQ14_B	20	DQS0_A_c	86	Vss	152	CA6_B	218	DQ15_B
21	Vss	87	DQ28_A	153	Vss	219	Vss	22	DQS0_A_t	88	DQ29_A	154	Vss	220	Vss
23	DQ4_A	89	Vss	155	CA5_B	221	DQ16_B	24	Vss	90	Vss	156	CA4_B	222	DQ17_B
25	Vss	91	DQ30_A	157	CA3_B	223	Vss	26	DQ5_A	92	DQ31_A	158	CA2_B	224	Vss
27	DQ6_A	93	Vss	159	Vss	225	DQ18_B	28	Vss	94	Vss	160	Vss	226	DQ19_B
29	Vss	95	CB0_A	161	CS0_B_n	227	Vss	30	DQ7_A	96	CB1_A	162	CA1_B	228	Vss
31	DQ8_A	97	Vss	163	RESET_n	229	DM2_B_n	32	Vss	98	Vss	164	CA0_B	230	DQS2_B_c
33	Vss	99	CB2_A	165	CS1_B_n	231	Vss	34	DQ9_A	100	DQS4_A_c	166	Vss	232	DQS2_B_t
35	DQ10_A	101	Vss	167	Vss	233	DQ20_B	36	Vss	102	DQS4_A_t	168	CB0_B	234	Vss
37	Vss	103	CB3_A	169	DQS4_B_c	235	Vss	38	DQ11_A	104	Vss	170	Vss	236	DQ21_B
39	DQS1_A_c	105	Vss	171	DQS4_B_t	237	DQ22_B	40	Vss	106	CS0_A_n	172	CB1_B	238	Vss
41	DQS1_A_t	107	CA0_A	173	Vss	239	Vss	42	DM1_A_n	108	ALERT_n	174	Vss	240	DQ23_B
43	Vss	109	CA1_A	175	CB3_B	241	DQ24_B	44	Vss	110	CS1_A_n	176	CB2_B	242	Vss
45	DQ12_A	111	Vss	177	Vss	243	Vss	46	DQ13_A	112	Vss	178	Vss	244	DQ25_B
47	Vss	113	CA2_A	179	DQ0_B	245	DQ26_B	48	Vss	114	CA3_A	180	DQ1_B	246	Vss
49	DQ14_A	115	CA4_A	181	Vss	247	Vss	50	DQ_15_A	116	CA5_A	182	Vss	248	DQ27_B
51	Vss	117	Vss	183	DQ2_B	249	DQS3_B_c	52	Vss	118	Vss	184	DQ3_B	250	Vss
53	DQ16_A	119	CA6_A	185	Vss	251	DQS3_B_t	54	DQ17_A	120	CA7_A	186	Vss	252	DM3_B_n
55	Vss	121	CA8_A	187	DM0_B_n	253	Vss	56	Vss	122	CA9_A	188	DQS0_B_c	254	Vss
57	DQ18_A	123	Vss	189	Vss	255	DQ28_B	58	DQ19_A	124	Vss	190	DQS0_B_t	256	DQ29_B
59	Vss	125	CA10_A	191	DQ4_B	257	Vss	60	Vss	126	CA11_A	192	Vss	258	Vss
61	DM2_A_n	127	CA12_A	193	Vss	259	DQ30_B	62	DQS2_A_c	128	RFU	194	DQ5_B	260	DQ31_B
63	Vss	129	Vss	195	DQ6_B	261	Vss	64	DQS2_A_t	130	Vss	196	Vss	262	Vss
65	DQ20_A	131	CK0_A_t	197	Vss			66	Vss	132	CK1_A_t	198	DQ7_B		

6. Block Diagram



Thermal Characteristics

Symbol	Parameter		Rating	Units	Note
T_c	Operation Temperature	Normal Operating Temp.	0 to 85	°C	1,2,3
		Extended Temp.	85 to 95	°C	1,2,3,4
T_{STG}	Storage Temperature		-55 to 100	°C	5
HSTG	Non-operating storage relative humidity (non-condensing)		5 to 95	%	

Note:
1. Maximum operating case temperature; Tc is measured in the center of the package.
2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum Tc during operation.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum Tc during operation.
4. If Tc exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 1.95µs interval refresh rate.
5. Storage temperature is defined as the temperature of the top/center of the DRAM and does not reflect the storage temperatures of shipping trays.

7. IDD, IDDQ and IPP Specifications

Symbol	Description	Value (Typical)		Units
		I_{DD} Max.	I_{PP} Max.	
IDD0	Operating One Bank Active-Precharge Current	1840	80	mA
IDD0F	Operating Four Bank Active-Precharge Current	2056	96	mA
IDD2N	Precharge Standby Current	1720	88	mA
IDD2P	Precharge Power-Down Current	1680	64	mA
IDD3N	Active Standby Current	2160	104	mA
IDD3P	Active Power-Down Current	2160	104	mA
IDD4R	Operating Burst Read Current	3440	96	mA
IDD4W	Operating Burst Write Current	3808	320	mA
IDD5B	Burst Refresh Current (Normal Refresh Mode)	3232	280	mA
IDD5C	Burst Refresh Current (Same Bank Refresh Mode)	2184	128	mA
IDD6N	Self Refresh Current: Normal Temperature Range	1752	256	mA
IDD6E	Self Refresh Current: Extended Temperature Range	2448	296	mA
IDD7	Operating Bank Interleave Read Current	4240	200	mA
IDD8	Maximum Power Saving Deep Power Down Current	1712	96	mA

8. Timing Parameters

Parameter	Symbol	4400		4800		5200		Unit
		Min	Max	Min	Max	Min	Max	
Clock Timing								
Average clock period	tCK,AVG	0.454	<0.500	0.416	<0.454	0.384	<0.416	ns
Command and Address Timing								
Read to Read command delay for same bank group	tCCD_L	8nCK,5ns (MAX)		8nCK,5ns (MAX)		8nCK,5ns (MAX)		nCK
WRITE to WRITE command delay for same bank group	tCCD_L_WR	32nCK, 20ns (MAX)		32nCK, 20ns (MAX)		32nCK, 20ns (MAX)		nCK
WRITE to WRITE command delay for same bank group, second WRITE not RMW	tCCD_L_WR2	16nCK, 10ns (MAX)		16nCK, 10ns (MAX)		16nCK, 10ns (MAX)		nCK
Read to Read or Write to Write command delay for different bank group for BL16, BC8 OTF	tCCD_S	8		8		8		nCK
ACTIVATE to ACTIVATE command delay to different bank group for 2KB page size	tRRD_S,2K	8		8		8		nCK
ACTIVATE to ACTIVATE command delay to different bank group for 1KB page size	tRRD_S,1K	8		8		8		nCK
ACTIVATE to ACTIVATE command delay to same bank group for 2KB page size	tRRD_L,2K	8nCK,5ns (MAX)		8nCK,5ns (MAX)		8nCK,5ns (MAX)		nCK
ACTIVATE to ACTIVATE command delay to same bank group for 1KB page size	tRRD_L,1K	8nCK,5ns (MAX)		8nCK,5ns (MAX)		8nCK,5ns (MAX)		nCK
Four activate window for 2KB page size	tFAW,2K	40nCK, 18.160ns (MAX)		40nCK, 16.640ns (MAX)		40nCK, 15.360ns (MAX)		ns
Four activate window for 1KB page size	tFAW,1K	32nCK, 14.528ns (MAX)		32nCK, 13.312ns (MAX)		32nCK, 12.288ns (MAX)		ns
Delay from start of internal WRITE transaction to internal READ command for different bank group	tWTR_S	4nCK, 2.5ns (MAX)		4nCK, 2.5ns (MAX)		4nCK, 2.5ns (MAX)		ns

Delay from start of internal WRITE transaction to internal READ command for same bank group	tWTR_L	16nCK, 10ns (MAX)		16nCK, 10ns (MAX)		16nCK, 10ns (MAX)		ns
Delay from start of internal WRITE transaction to internal READ with AUTO PRECHARGE command for same bank	tWTRA	tWR-tRTP		tWR-tRTP		tWR-tRTP		ns
Internal READ command to PRECHARGE command delay	tRTP	12nCK, 7.5ns (MAX)		12nCK, 7.5ns (MAX)		12nCK, 7.5ns (MAX)		ns
PRECHARGE to PRECHARGE delay	tPPD	2		2		2		nCK
WRITE recovery time	tWR	29.964		29.952		29.952		ns
DLL locking time	tDLLK	1280		1536		1536		nCK
Mode Register Read/Write Timing								
Mode register READ command period	tMRR	14ns, 16nCK (MAX)		14ns, 16nCK (MAX)		14ns, 16nCK (MAX)		
Mode register READ pattern to mode register READ pattern command spacing	tMRR_p	8		8		8		nCK
Mode register WRITE command period	tMRW	5ns,8nCK (MAX)		5ns,8nCK (MAX)		5ns,8nCK (MAX)		
Mode register SET command delay	tMRD	14ns, 16nCK (MAX)		14ns, 16nCK (MAX)		14ns, 16nCK (MAX)		
DFE mode register WRITE update delay time	tDFE	80		80		80		ns
Data Strobe Timing								
DQS_t, DQS_c differential READ preamble	tRPRE	TBD		TBD		TBD		tCK
DQS_t, DQS_c differential READ postamble	tRPST	TBD		TBD		TBD		tCK
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c	tDQSCK	-0.286	0.286	-0.3	0.3	TBD	TBD	tCK
DQS_t, DQS_c rising edge output variance window	tDQSCKI		0.475		0.49		TBD	tCK
Data Strobe Timing								
2-tCK WRITE preamble enable window	tWPRE_EN_2 tCK	1.5		1.5		1.5		tCK
3-tCK WRITE preamble enable window	tWPRE_EN_3 tCK	2.5		2.5		2.5		tCK
4-tCK WRITE preamble	tWPRE_EN_4	2.5		2.5		2.5		tCK

enable window	tCK							
DQS_t, DQS_c differential WRITE postamble	tWPST	TBD		TBD		TBD		tCK
Final trained value of host DQS_t-DQS_c timing relative to CWL CK_t-CK_c edge	tDQSoffset	-0.5	0.5	-0.5	0.5	-0.5	0.5	tCK
Write leveling setup time	tWLS	-80	80	-80	80	-80	80	ps
Write leveling hold time	tWLH	-80	80	-80	80	-80	80	ps
Voltage/temperature drift window of first rising DQS_t preamble edge relative to CWL CK_t-CK_c edge (x4/x8/x16)	tDQSD	-0.25 x tWPRE_EN_ntCK	0.25 x tWPRE_EN_ntCK	-0.25 x tWPRE_EN_ntCK	0.25 x tWPRE_EN_ntCK	-0.25 x tWPRE_EN_ntCK	0.25 x tWPRE_EN_ntCK	tCK
Host and system voltage/ temperature drift window of first rising DQS_t preamble edge relative to CWL CK_t-CK_c edge (x4/x8/x16)	tDQSS	-0.25 x tWPRE_EN_ntCK						tCK
MPSM Timing								
MPSM exit to first valid command delay	tMPSMX	tMRD		tMRD		tMRD		ns
ZQ Calibration Timing								
ZQ calibration time	tZQCAL	1		1		1		µs
ZQ calibration latch time	tZQLAT	30ns, 8nCK (MIN)		30ns, 8nCK (MIN)		30ns, 8nCK (MIN)		
Reset Timing								
RESET_n low time for reset initialization with stable power	tPW_RESET	1		1		1		µs
Time after RESET_n assertion to ODT off	tRST_ADC		50		50		50	ns
Self Refresh Timing								
Command pass disable delay	tCPDED	5ns,8nCK (MAX)		5ns,8nCK (MAX)		5ns,8nCK (MAX)		
Self refresh CS_n low pulse width	tCSL	10		10		10		ns
Self refresh exit CS_n high pulse width	tCSH_Srexit	13	30	13	30	13	30	ns
Self refresh exit CS_n low pulse width	tCSL_Srexit	3nCK	30ns	3nCK	30ns	3nCK	30ns	
Self refresh exit CS_n low pulse width with frequency change	tCSL_FreqChg	VREFCA_time		VREFCA_time		VREFCA_time		ns
Valid clock equirement before SRX	tCKSRX	3.5ns, 8nCK (MAX)		3.5ns, 8nCK (MAX)		3.5ns, 8nCK (MAX)		ns

Valid clock requirement after SRE	tCKLCS	tCPDED + 1nCK		tCPDED + 1nCK		tCPDED + 1nCK		nCK
Self refresh exit CS_n HIGH	tCASRX	0		0		0		ns
Exit self refresh to commands not requiring a locked DLL	tXS	tRFC1		tRFC1		tRFC1		ns
Exit self refresh to commands requiring a locked DLL	tXS_DLL	tDLLK		tDLLK		tDLLK		ns
Power-Down Timing								
Command pass disable delay	tCPDED	5ns,8nCK (MAX)		5ns,8nCK (MAX)		5ns,8nCK (MAX)		ns
Power-down time	tPD	7.5ns, 8nCK (MAX)	5*tREFI1 (normal) 9*tREFI2 (FGR)	7.5ns, 8nCK (MAX)	5*tREFI1 (normal) 9*tREFI2 (FGR)	7.5ns, 8nCK (MAX)	5*tREFI1 (normal) 9*tREFI2 (FGR)	ns
Exit power-down to next valid command	tXP	7.5ns, 8nCK (MAX)		7.5ns, 8nCK (MAX)		7.5ns, 8nCK (MAX)		ns
Timing of ACT command to POWER DOWN ENTRY command	tACTPDEN	2		2		2		nCK
Timing of PREab, PREsb or PREpb command to POWER DOWN ENTRY command	tPRPDEN	2		2		2		nCK
Timing of READ or READ w/ AP command to POWER DOWN ENTRY command	tRDPDEN	CL +RBL/2+1		CL +RBL/2+1		CL +RBL/2+1		nCK
Timing of WRITE command to POWER DOWN ENTRY command	tWRPDEN	CWL +WBL/ 2+ (tWR/ tCK(avg)) +1		CWL +WBL/ 2+ (tWR/ tCK(avg)) +1		CWL +WBL/ 2+ (tWR/ tCK(avg)) +1		nCK
Timing of WRITE w/ AP command to POWER DOWN ENTRY command	tWRAPDEN	CWL +WBL/ 2+-0.25 x tWPRE_EN_n tCKWR+1		CWL +WBL/ 2+-0.25 x tWPRE_EN_n tCKWR+1		CWL +WBL/ 2+-0.25 x tWPRE_EN_n tCKWR+1		nCK
Timing of REFab or REFsb command to POWER DOWN ENTRY command	tREFPDEN	2		2		2		nCK
Timing of MRR command to POWER DOWN ENTRY command	tMRRPDEN	CL+8+1		CL+8+1		CL+8+1		nCK
Timing of MRW command to POWER DOWN ENTRY command	tMRWPDEN	tMRD (MIN)		tMRD (MIN)		tMRD (MIN)		nCK
Timing of MPC command to POWER	tMPCPDEN	tMPC_delay		tMPC_delay		tMPC_delay		nCK

DOWN ENTRY command								
MPC Command Timing								
MPC to any other valid command	tMPC_Delay	tMRD		tMRD		tMRD		nCK
Time between stable MPC command and first falling CS edge (setup)	tMC_MPC_Setup	3		3		3		nCK
Time between first rising CS edge and stable MPC command (HOLD)	tMC_MPC_Hold	3		3		3		nCK
Time CS_n is held LOW to register MPC command	tMPC_CS	3.5	8	3.5	8	3.5	8	nCK
PDA Timing								
PDA ENUMERATE ID command to any other command cycle	tPDA_DELAY	tPDA_DQS_DELAY (MAX) + BL/2 + 19ns		tPDA_DQS_DELAY (MAX) + BL/2 + 19ns		TBD		ns
Delay to rising strobe edge used for sampling DQ during PDA operation	tPDA_DQS_DELAY	5	18	5	18	TBD	TBD	ns
DQS setup time during PDA operation	tPDA_S	3		3		TBD		nCK
DQS hold time during PDA operation	tPDA_H	3		3		TBD		nCK
Read Training Timing								
Registration of MRW continuous burst mode exit to next valid command delay	tCont_Exit_Delay		tCont_Exit + tMRW		tCont_Exit + tMRW		tCont_Exit + tMRW	ns
Registration of MRW continuous burst mode exit to end of training mode	tCont_Exit		CL+BL/ 2+10nCK		CL+BL/ 2+10nCK		CL+BL/ 2+10nCK	ns
Read Preamble Timing								
Delay from MRW command to DQS driven	tSDOn		12nCK, 20ns (MAX)		12nCK, 20ns (MAX)		12nCK, 20ns (MAX)	
Delay from MRW command to DQS disabled	tSDOff		12nCK, 20ns (MAX)		12nCK, 20ns (MAX)		12nCK, 20ns (MAX)	
CA Training Mode Timing								
Registration of CAM entry command to start of training samples time	tCATM_Entry	20		20		20		ns
Registration of CATM exit CS_n assertion to end of training mode (when DQ is	tCATM_Exit		14		14		14	ns

no longer driven by the device).								
Registration of CATM exit to next valid command delay	tCATM_Exit_ Delay	20		20		20		ns
Time from sample evaluation to output on DQ bus	tCATM_Valid		20		20		20	ns
Time output is available on DQ bus	tCATM_DQ_ Window	2		2		2		nCK
CS_n assertion duration to exit CATM	tCATM_CS_E xit	2	8	2	8	2	8	nCK
Registration of CSTM entry command to start of training samples time	tCSTM_Entry	20		20		20		ns
Min time between last CS_n pulse and first pulse of MPC command to exit CSTM	tCSTM_Min_ to_MPC_exit	4		4		4		nCK
Registration of CSTM exit command to end of training mode	tCSTM_Exit		20		20		20	ns
Time from sample evaluation to output on DQ bus	tCSTM_Valid		20		20		20	ns
Time output is available on DQ bus	tCSTM_DQ_ Window	2		2		2		nCK
Registration of CSTM exit to next valid command delay	tCSTM_Exit_ Delay	20		20		20		ns
Write Leveling Timing								
Write leveling pulse enable: time from write leveling training enable MRW to when internal write leveling pulse logic level is valid	tWLPEN	0	15	0	15	0	15	ns
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	ns
Write leveling output error	tWLOE	0	2	0	2	0	2	ns
Width of write leveling internal pulse	tWL_Pulse_ Width	2		2		2		tCK
VREFCA/VREFCS Timing								
VREFCA/VREFCS command to any other valid command delay	tVREFCA_Delay/ tVREFCS_Delay	tMRD		tMRD		tMRD		nCK
Time CS_n is held LOW to register VREFCA/VREFCS	tVREFCA_CS/ tVREFCS_CS	3.5	8	3.5	8	3.5	8	nCK

command								
hPPR/sPPR Timing								
hPPR programming time (x4/x8)	tPGMa	1000		1000		1000		ms
hPPR programming time (x16)	tPGMb	2000		2000		2000		ms
sPPR programming time	tPGM_sPPR	CWL +8tCK +tWR		CWL +8tCK +tWR		CWL +8tCK +tWR		tCK
hPPR/sPPR recognition time	tPGM_Exit	tRP		tRP		tRP		ns
hPPR program exit and new address setting time	tPGMPST	50		50		50		µs
sPPR program exit and new address setting time	tPGMPST_sPPR	tMRD		tMRD		tMRD		ns
DQS Interval Oscillator Readout Timing								
Delay time from DQS interval oscillator stop to mode register readout	tOSCO	tMPC_Delay		tMPC_Delay		tMPC_Delay		nCK
DQS interval oscillator start gap in automatic stop mode	tOSCS	tMPC_Delay + DQS interval timer runtime						nCK
ECS Timing								
ECS operation time	tECSc	176nCK, 110ns (MAX)		176nCK, 110ns (MAX)		176nCK, 110ns (MAX)		
CRC Error Reporting Timing								
CRC error to ALERT n_latency	tCRC_ALERT	3	13	3	13	3	13	ns
CRC ALERT_n pulse width	CRC_ALERT_PW	12	20	12	20	12	20	nCK

9. SPD

Byte Number	Function Described	Function supported	Hex Value
0	Number of Bytes in SPD Device	1024 Bytes	30
1	SPD Revision for Base Configuration Parameters	Revision 1.0	10
2	Key Byte / Host Bus Command Protocol Type	DDR5 SDRAM	12
3	Key Byte / Module Type	SODIMM	03
4	First SDRAM Density and Package	Monolithic 24Gb	05
5	First SDRAM Addressing	10 columns/17 rows	01
6	First SDRAM I/O Width	x8	20
7	First SDRAM Bank Groups & Banks Per Bank Group	8BGs / 4Banks per BG	62
8	Second SDRAM Density and Package	N/A	00
9	Second SDRAM Addressing	N/A	00
10	Second SDRAM I/O Width	N/A	00
11	Second SDRAM Bank Groups & Banks Per Bank Group	N/A	00
12	SDRAM BL32 & Post Package Repair	BL32 not / sPPR supported / MBIST/mPPR supported	A2
13	SDRAM Duty Cycle Adjuster & Partial Array Self Refresh	PASR supported	12
14	SDRAM Fault Handling	supported	0F
15	Reserved	Reserved	00
16	SDRAM Nominal Voltage, VDD	1.1V	00
17	SDRAM Nominal Voltage, VDDQ	1.1V	00
18	SDRAM Nominal Voltage, VPP	1.8V	00
19	SDRAM Timing	Standard	00
20	SDRAM Minimum Cycle Time (t_{CKAVG}min), Least Significant Byte	357ps	65
21	SDRAM Minimum Cycle Time (t_{CKAVG}min), Most Significant Byte	357ps	01
22	SDRAM Maximum Cycle Time (t_{CKAVG}max), Least Significant Byte	1010ps	F2
23	SDRAM Maximum Cycle Time (t_{CKAVG}max), Most Significant Byte	1010ps	03
24	CAS Latencies Supported, First Byte	22,26,28,30,32,36,40,42,46,50	7A
25	CAS Latencies Supported, Second Byte	22,26,28,30,32,36,40,42,46,50	AD
26	CAS Latencies Supported, Third Byte	22,26,28,30,32,36,40,42,46,50	00
27	CAS Latencies Supported, Fourth Byte	22,26,28,30,32,36,40,42,46,50	00
28	CAS Latencies Supported, Fifth Byte	22,26,28,30,32,36,40,42,46,50	00
29	Reserved	Reserved	00
30	SDRAM Minimum CAS Latency Time (t_{AA}min), Least Significant Byte	16000ps	80
31	SDRAM Minimum CAS Latency Time (t_{AA}min), Most Significant Byte	16000ps	3E
32	SDRAM Minimum RAS to CAS Delay Time (t_{RCD}min), Least Significant Byte	16000ps	80
33	SDRAM Minimum RAS to CAS Delay Time (t_{RCD}min), Most Significant Byte	16000ps	3E
34	SDRAM Minimum Row Precharge Delay Time (t_{RP}min), Least Significant Byte	16000ps	80
35	SDRAM Minimum Row Precharge Delay Time (t_{RP}min), Most Significant Byte	16000ps	3E

36	SDRAM Minimum Active to Precharge Delay Time (t_{RAS}min), Least Significant Byte	32000ps	00
37	SDRAM Minimum Active to Precharge Delay Time (t_{RAS}min), Most Significant Byte	32000ps	7D
38	SDRAM Minimum Active to Active/Refresh Delay Time (t_{RC}min), Least Significant Byte	48000os	80
39	SDRAM Minimum Active to Active/Refresh Delay Time (t_{RC}min), Most Significant Byte	48000os	BB
40	SDRAM Minimum Write Recovery Time (t_{WR}min), Least Significant Byte	30000ps	30
41	SDRAM Minimum Write Recovery Time (t_{WR}min), Most Significant Byte	30000ps	75
42	SDRAM Minimum Refresh Recovery Delay Time (t_{RFC1}min, t_{RFC1}_slr min), Least Significant Byte	410ns	9A
43	SDRAM Minimum Refresh Recovery Delay Time (t_{RFC1}min, t_{RFC1}_slr min), Most Significant Byte	410ns	01
44	SDRAM Minimum Refresh Recovery Delay Time (t_{RFC2}min, t_{RFC2}_slr min), Least Significant Byte	220ns	DC
45	SDRAM Minimum Refresh Recovery Delay Time (t_{RFC2}min, t_{RFC2}_slr min), Most Significant Byte	220ns	00
46	SDRAM Minimum Refresh Recovery Delay Time (t_{RFCsb}min, t_{RFCsb}_slr min), Least Significant Byte	190ns	BE
47	SDRAM Minimum Refresh Recovery Delay Time (t_{RFCsb}_dlr min), Most Significant Byte	190ns	00
48	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFC1}_dlr min), Least Significant Byte	N/A	00
49	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFC1}_dlr min), Most Significant Byte	N/A	00
50	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFC2}_dlr min), Least Significant Byte	N/A	00
51	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFC2}_dlr min), Most Significant Byte	N/A	00
52	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFCsb}_dlr min), Least Significant Byte	N/A	00
53	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFCsb}_dlr min), Most Significant Byte	N/A	00
54	SDRAM Refresh Management, First Byte, First SDRAM	N/A	D4
55	SDRAM Refresh Management, Second Byte, First SDRAM	N/A	00
56	SDRAM Refresh Management, First Byte, Second SDRAM	N/A	00
57	SDRAM Refresh Management, Second Byte, Second SDRAM	N/A	00
58	SDRAM Adaptive Refresh Management Level A, First Byte, First SDRAM	N/A	D4
59	SDRAM Adaptive Refresh Management Level A, Second Byte, First SDRAM	N/A	00
60	SDRAM Adaptive Refresh Management Level A, First Byte, Second SDRAM	N/A	00
61	SDRAM Adaptive Refresh Management Level A, Second Byte, Second SDRAM	N/A	00
62	SDRAM Adaptive Refresh Management Level B, First Byte, First SDRAM	N/A	D4
63	SDRAM Adaptive Refresh Management Level B, Second Byte, First SDRAM	N/A	00
64	SDRAM Adaptive Refresh Management Level B, First Byte, Second SDRAM	N/A	00
65	SDRAM Adaptive Refresh Management Level B, Second Byte, Second SDRAM	N/A	00
66	SDRAM Adaptive Refresh Management Level C, First Byte, First SDRAM	N/A	D4
67	SDRAM Adaptive Refresh Management Level C, Second Byte, First SDRAM	N/A	00
68	SDRAM Adaptive Refresh Management Level C, First Byte, Second SDRAM	N/A	00
69	SDRAM Adaptive Refresh Management Level C, Second Byte, Second SDRAM	N/A	00
70	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group (t_{RRD_L}min), Least Significant Byte	5000ps	88
71	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group (t_{RRD_L}min), Most Significant Byte	5000ps	13

72	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group (t_{RRD_L}min), Lower Clock Limit	8nCK	08
73	SDRAM Minimum CAS_n to CAS_n Command Delay Time, Same Bank Group (tCCD_Lmin), Least Significant Byte	5000ps	88
74	SDRAM Minimum CAS_n to CAS_n Command Delay Time, Same Bank Group (tCCD_Lmin), Most Significant Byte	5000ps	13
75	SDRAM Minimum CAS_n to CAS_n Command Delay Time, Same Bank Group (tCCD_Lmin), Lower Clock Limit	8nCK	08
76	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group ($t_{CCD_L_WR}$min), Least Significant Byte	20000ps	20
77	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group ($t_{CCD_L_WR}$min), Most Significant Byte	20000ps	4E
78	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group ($t_{CCD_L_WR}$min), Lower Clock Limit	32nCK	20
79	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Second Write not RMW, Same Bank Group ($t_{CCD_L_WR2}$min), Least Significant Byte	10000ps	10
80	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Second Write not RMW, Same Bank Group ($t_{CCD_L_WR2}$min), Most Significant Byte	10000ps	27
81	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Second Write not RMW, Same Bank Group ($t_{CCD_L_WR2}$min), Lower Clock Limit	16nCK	10
82	SDRAM Minimum Four Activate Window (t_{FAW}min), Least Significant Byte	11428ps	A4
83	SDRAM Minimum Four Activate Window (t_{FAW}min), Most Significant Byte	11428ps	2C
84	SDRAM Minimum Four Activate Window (t_{FAW}min), Lower Clock Limit	32nCK	20
85	SDRAM Minimum Internal Write to Read Command Delay Time, Same Bank Group, (t_{WTR_L}min), Least Significant Byte	10000ps	10
86	SDRAM Minimum Internal Write to Read Command Delay Time, Same Bank Group, (t_{WTR_L}min), Most Significant Byte	10000ps	27
87	SDRAM Minimum Internal Write to Read Command Delay Time, Same Bank Group, (t_{WTR_L}min), Lower Clock Limit	16nCK	10
88	SDRAM Minimum Internal Write to Read Command Delay Time, Different Bank Group, (t_{WTR_S}min), Least Significant Byte	2500ps	C4
89	SDRAM Minimum Internal Write to Read Command Delay Time, Different Bank Group, (t_{WTR_S}min), Most Significant Byte	2500ps	09
90	SDRAM Minimum Internal Write to Read Command Delay Time, Different Bank Group, (t_{WTR_S}min), Lower Clock Limit	4nCK	04
91	SDRAM Minimum Internal Read to Precharge Command Delay Time, (t_{RTP}min), Least Significant Byte	7500ps	4C
92	SDRAM Minimum Internal Read to Precharge Command Delay Time, (t_{RTP}min), Most Significant Byte	7500ps	1D
93	SDRAM Minimum Internal Read to Precharge Command Delay Time, (t_{RTP}min), Lower Clock Limit	12nCK	0C
94~127	Reserved -- must be coded as 0x00	Reserved	00
128~191	Reserved for future use	Reserved	00
192	SPD Revision for SPD bytes 192~447	Revision 1.0	10
193	Hashing Sequence	No authentication	00
194	SPD Manufacturer ID Code, First Byte	Montage	86
195	SPD Manufacturer ID Code, Second Byte	Montage	32
196	SPD Device Type	Montage	80
197	SPD Device Revision Number	Montage	15
198	PMIC 0 Manufacturer ID Code, First Byte	Richtek	8A
199	PMIC 0 Manufacturer ID Code, Second Byte	Richtek	8C
200	PMIC 0 Device Type	Richtek	82
201	PMIC 0 Revision Number	Richtek	13

202	PMIC 1 Manufacturer ID Code, First Byte	N/A	00
203	PMIC 1 Manufacturer ID Code, Second Byte	N/A	00
204	PMIC 1 Device Type	N/A	00
205	PMIC 1 Revision Number	N/A	00
206	PMIC 2 Manufacturer ID Code, First Byte	N/A	00
207	PMIC 2 Manufacturer ID Code, Second Byte	N/A	00
208	PMIC 2 Device Type	N/A	00
209	PMIC 2 Revision Number	N/A	00
210	Thermal Sensor Manufacturer ID Code, First Byte	N/A	00
211	Thermal Sensor Manufacturer ID Code, Second Byte	N/A	00
212	Thermal Sensor Device Type	N/A	00
213	Thermal Sensor Revision Number	N/A	00
214	DRAM Specification Level	Reserved	00
215	SPD Specification Level	N/A	00
216	PMIC0 Specification Level	N/A	00
217	PMIC1 Specification Level	N/A	00
218	PMIC2 Specification Level	N/A	00
219	TS Specification Level	N/A	00
220	DIMM Specification Level	N/A	00
221~229	Reserved	Reserved	00
230	Module Nominal Height	29 < height <= 30 mm	0F
231	Module Maximum Thickness	1 < thickness <= 2 mm	01
232	Reference Raw Card Used	R/C A rev 0	00
233	DIMM Attributes	Tc 0 to +95 °C, 2rows	82
234	Module Organization	Symmetrical 1 Package Rank	00
235	Memory Channel Bus Width	2 channels, 32 bits per channel	22
236~239	Reserved	Reserved	00
240~447	Reserved	Reserved	00
448~509	Reserved for future use	Reserved	00
510~511	CRC for SPD bytes 0~509	CRC	F3 B4
512	Module Manufacturer ID Code, First Byte	Advantech	8A
513	Module Manufacturer ID Code, Second Byte	Advantech	C8
514	Module Manufacturing Location	Made in Taiwan	02
515~516	Module Manufacturing Date		-
517~520	Module Serial Number		-
521~550	Module Part Number	SQR-SD5N24G5K6M	53 51 52 2D 53 44 35 4E 32 34 47 35 4B 36 4D 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20
551	Module Revision Code		00

552	DRAM Manufacturer ID Code, First Byte	Micron	80
553	DRAM Manufacturer ID Code, Second Byte	Micron	2C
554	DRAM Stepping		00
555~639	Manufacturer's Specific Data		-
640~703	End User Programmable	Reserved	00
704~767	End User Programmable	Reserved	00
768~831	End User Programmable	Reserved	00
832~895	End User Programmable	Reserved	00
896~959	End User Programmable	Reserved	00
960~1023	End User Programmable	Reserved	00

Appendix: Part Number Table

Product	Advantech PN
SQRAM 24GB SO-DDR5-5600 3Gx8 Micron (0~95)	**SSQR-SD5N24G5K6M**