

M.2 22110 PCIe SSD 920 Datasheet

(SQF-CMBxx-xG-ECx)

Revision History

Rev.	Date	History
0.1	2019/12/27	1. Preliminary release
0.2	2020/2/20	1. Updated product information
0.3	2024/07/09	1. Modify SMART information

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1. Overview

Advantech SQFlash 920 series M.2 22110 PCIe SSD (Solid State Drive) delivers all the advantages of flash disk technology with PCIe Gen3 x4 interface and is fully compliant with the standard Next Generation Form Factor (NGFF) called M.2 Card Format. SQF-CMB 920 22110 offers a wide range capacities up to 3840GB and its performance can reach up to 3200 MB/s¹ (for read) and 1000 MB/s¹ (for write) based on Toshiba BiCS3 TLC NAND flash with the choice of 512MB/1GB/2GB/4GB DDR4. Moreover, the power consumption of SQF-CMB 920 M.2 22110 is much lower than traditional hard drives, making it the best embedded solution for new platforms.

NOTE:

1. From Oct 2019, Toshiba Memory officially changed company's name to Kioxia
2. Achieved by 3840GB SSD with external 2GB DDR4 at FOB (fresh-out-of-box) state on CrystalDiskMark V6.0
3. The choice of DDR4 depends on drive capacity; DDR size = 0.1% of SSD capacity.

2. Features

■ PCIe Interface

- Compliant with NVMe1.3
- Compatible with PCIe I/II/III x4 interface
- PCIe Gen 3 x 4 lane & backward compatible to PCIe Gen 2 and Gen 1
- 8 IO queues supported(1 admin queue and 8 IO queue). Each IO queue support 256 entries.

■ Operating Voltage : 3.3V

■ Support LDPC with RAID ECC

■ AES256 、TCG-OPAL 、TRIM 、AHCI supported

■ Hardware Quick Erase supported (optional)

■ Voltage Stabilizer supported (optional)

■ Temperature Ranges¹

- Commercial Temperature
 - 0°C to 70°C for operating
 - -40°C to 85°C for storage
- Industrial Temperature
 - -40°C to 85°C for operating
 - -40°C to 85°C for storage

*Note : 1. Based on SMART Attribute (Byte index [2 :1] of PCIe-SIG standard, which measured by thermal sensor

■ Mechanical Specification

- Shock : 1,500G / 0.5ms
- Vibration : 20G / 80~2,000Hz

■ Humidity

- Humidity : 5% ~ 95% under 55°C

■ Acquired RoHS 、WHQL 、CE 、FCC Certificate

■ Acoustic : 0 dB

■ Dimension : 110.0 mm x 22.0 mm x 7.3 mm

3. Specification Table

■ Performance

		Sequential (MB/sec)		Random (IOPS @4K)	
		Read	Write	Read	Write
3D TLC	480 GB	3000.00	580.00	TBD	TBD
	960 GB	3200.00	1000.00	TBD	TBD
	1920 GB	2700.00	1000.00	TBD	TBD
	3840 GB	2600.00	950.00	TBD	TBD

1. From Oct 2019, Toshiba Memory officially changed company's name to Kioxia
2. The performance was estimated based on Kioxia¹ BiCS3 TLC NAND flash.
3. Performance may differ according to flash configuration and platform.
4. The tables are for reference only. Any criteria for accepting goods shall be further discussed based on different flash configurations.
5. Performance is measured with the following conditions
 - (a) CrystalDiskMark 6.0, 1GB range, QD=32, Thread=1
 - (b) IOMeter, 8GB range, 4K data size, QD=32

■ Endurance

JEDEC defined an endurance rating TBW (TeraByte Written), following by the equation below, for indicating the number of terabytes a SSD can be written which is a measurement of SSDs' expected lifespan, represents the amount of data written to the device.

$$\text{TBW} = [(\text{NAND Endurance}) \times (\text{SSD Capacity})] / \text{WAF}$$

- **NAND Endurance:** Program / Erase cycle of a NAND flash.
 - SLC: 100,000 cycles
 - Ultra MLC: 30,000 cycles
 - MLC: 3,000 cycles
 - 3D TLC (BiCS3): 3,000 cycles
- **SSD Capacity:** SSD physical capacity in total of a SSD.
- **WAF:** Write Amplification Factor (WAF), as the equation shown below, is a numerical value representing the ratio between the amount of data that a SSD controller needs to write and the amount of data that the host's flash controller writes. A better WAF, which is near to 1, guarantees better endurance and lower frequency of data written to flash memory.

$$\text{WAF} = (\text{Lifetime write to flash}) / (\text{Lifetime write to host})$$

Endurance measurement is based on JEDEC 219 workload and verified with following workload conditions,

- PreCond%full = 100%
- Trim commands enabled
- Random data pattern.

➤ SQFlash 920 M.2 22110 PCIe SSD TBW

	WAF	TBW
		3D TLC
480 GB	TBD	TBD
960 GB	TBD	TBD
1920 GB	TBD	TBD
3840 GB	1.85	6,200

* Subject to change based on firmware migration

4. General Description

■ Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, SQFlash 920 series PCIe SSD applies the LDPC with RAID ECC algorithm, which can detect and correct errors occur during read process, ensure data been read correctly, as well as protect data from corruption.

■ Wear Leveling

NAND flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some areas get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

SQFlash provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND flash is greatly improved.

■ Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. SQFlash implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

■ Power Loss Protection

– Flush Manager

Power Loss Protection is a mechanism to prevent data loss during unexpected power failure. DRAM is a volatile memory and frequently used as temporary cache or buffer between the controller and the NAND flash to improve the SSD performance. However, one major concern of the DRAM is that it is not able to keep data during power failure. Accordingly, SQFlash SSD applies the Flush Manager technology, only when the data is fully committed to the NAND flash will the controller send acknowledgement (ACK) to the host. Such implementation can prevent false-positive performance and the risk of power cycling issues.

In addition, it is critical for a controller to shorten the time the in-flight data stays in the controller internal cache. Thus, SQFlash applies an algorithm to reduce the amount of data resides in the cache to provide a better performance. With Flush Manager, incoming data would only have a “pit stop” in the cache and then move to NAND flash directly. Also, the onboard DDR will be treated as an “organizer” to consolidate incoming data into groups before written into the flash to improve write amplification.

– Voltage Stabilizer

While the built-in voltage detector detects an unstable power input ($< 3.135\text{ V}$ or $> 3.465\text{ V}$), the controller will issue a power failure interrupt and force a Flush CMD first. At the same time, the whole internal power supply will be switched to Voltage Stabilizer immediately to ensure stable power is supplied throughout the whole drive. This ensures the Flash IC and DDR IC will not operate with unstable power which could lead to data errors or bad data integrity.

■ TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid-state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD which blocks of data are no longer in use and can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks all the time.

■ SMART

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a hard disk drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

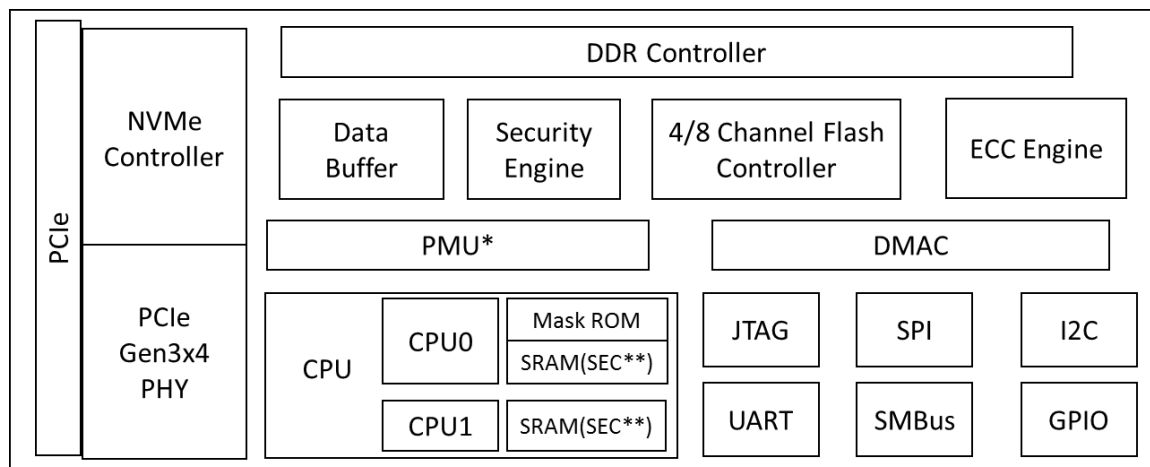
■ Over-Provision

Over Provisioning refers to the inclusion of extra NAND capacity in a SSD, which is not visible and cannot be used by users. With Over Provisioning, the performance and IOPS (Input/Output Operations per Second) are improved by providing the controller additional space to manage P/E cycles, which enhances the reliability and endurance as well. Moreover, the write amplification of the SSD becomes lower when the controller writes data to the flash.

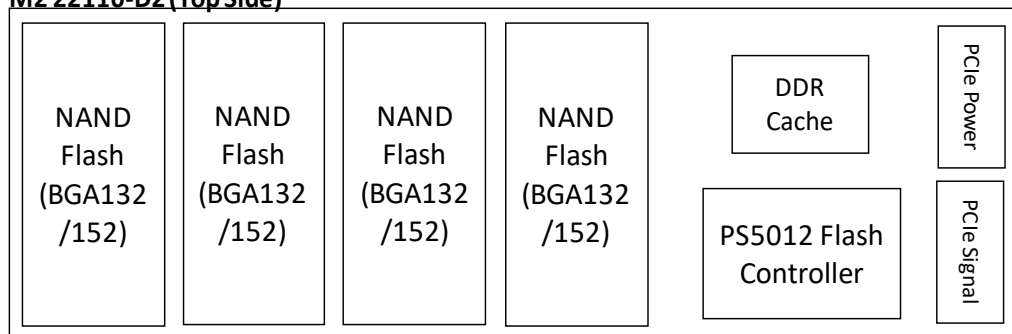
■ Thermal Throttling

Thermal Throttling function is for protecting the drive and reducing the possibility of read / write error due to overheat. The temperature is monitored by the thermal sensor. As the operating temperature continues to increase to threshold temperature, the Thermal Throttling mechanism is activated. At this time, the performance of the drive will be significantly decreased to avoid continuous heating. When the operating temperature falls below threshold temperature, the drive can resume to normal operation.

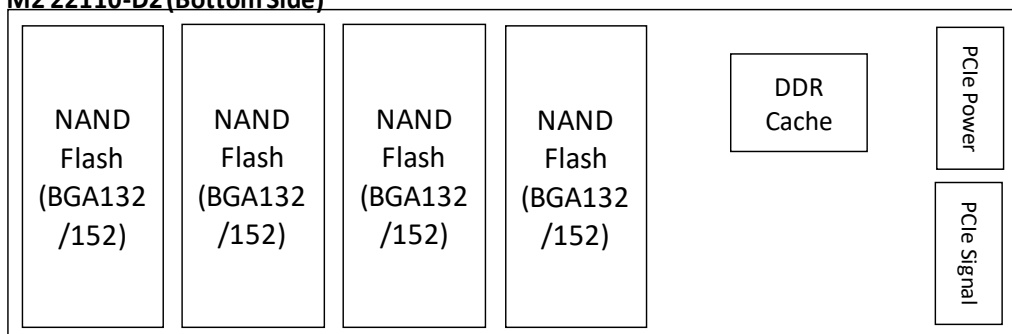
■ Block Diagram



M2 22110-D2 (Top Side)



M2 22110-D2 (Bottom Side)



■ LBA value

Density (GB)	LBA
480	TBD
960	TBD
1920	TBD
3840	7,501,476,528

5. Security Features

■ **Advanced Encryption Standard (AES)**

An AES 256-bit encryption key is generated in the drive's security controller before the data got stored on the NAND flash. When the controller or firmware fails, the data that is securely stored in the encryption key becomes inaccessible through the NAND flash.

■ **TCG-OPAL 2.0 Compliance**

TCG-OPAL compliance SED (Self-encryption Drive) supports a built-in shadow MBR to process user authentication to SSD before booting to normal MBR area and OS. SQFlash 920 series supports such feature with 100% TCG-OPAL compliance. Further, with SQFlash Flash Lock function, the user authentication process in shadow MBR can be done automatically by bonding with motherboard unique ID such as UUID in BIOS / MAC address / TPM unique code. So with Flash Lock enabled, only designated motherboard can have access to the SSD.

■ **Flash Vault**

Flash Vault is to lock Read and Write command by SSD firmware setting and make the SSD need password to verify and only operate with the corresponding platform. User can use Flash Vault to prevent data being stolen by reading the SQFlash SSD with other computers and unauthorized person.

■ **Security ID**

Security ID is to encrypt user's specific application software encryption. To enable this function, the application software is required to build Security ID function code and user needs to enable the firmware function by entering Access Code of SQFlash Utility, and then the Security ID can be set. When Security ID sets, the application software is protected by Security ID and SQFlash Utility

6. Pin Assignment and Description

Pin No.	PCIe Pin	Description
1	GND	CONFIG_3 = GND
2	3.3V	3.3V source
3	GND	Ground
4	3.3V	3.3V source
5	PETn3	PCIe TX Differential signal defined by the PCI Express M.2 spec
6	N/C	No connect
7	PETp3	PCIe TX Differential signal defined by the PCI Express M.2 spec
8	N/C	No connect
9	GND	Ground
10	LED1#	Open drain, active low signal. These signals are used to allow the add-in card to provide status indicators via LED devices that will be provided by the system.
11	PERn3	PCIe RX Differential signal defined by the PCI Express M.2 spec
12	3.3V	3.3V source
13	PERp3	PCIe RX Differential signal defined by the PCI Express M.2 spec
14	3.3V	3.3V source
15	GND	Ground
16	3.3V	3.3V source
17	PETn2	PCIe TX Differential signal defined by the PCI Express M.2 spec
18	3.3V	3.3V source
19	PETp2	PCIe TX Differential signal defined by the PCI Express M.2 spec
20	N/C	No connect
21	GND	Ground
22	N/C	No connect
23	PERn2	PCIe RX Differential signal defined by the PCI Express M.2 spec
24	N/C	No connect
25	PERp2	PCIe RX Differential signal defined by the PCI Express M.2 spec
26	N/C	No connect
27	GND	Ground
28	N/C	No connect
29	PETn1	PCIe TX Differential signal defined by the PCI Express M.2 spec

Pin No.	PCIe Pin	Description
30	N/C	No connect
31	PETp1	PCIe TX Differential signal defined by the PCI Express M.2 spec
32	N/C	No connect
33	GND	Ground
34	N/C	No connect
35	PERn1	PCIe RX Differential signal defined by the PCI Express M.2 spec
36	N/C	No connect
37	PERp1	PCIe RX Differential signal defined by the PCI Express M.2 spec
38	N/C	No connect
39	GND	Ground
40	SMB_CLK (I/O)(0/1.8V)	SMBus Clock; Open Drain with pull-up on platform
41	PETn0	PCIe TX Differential signal defined by the PCI Express M.2 spec
42	SMB_DATA (I/O)(0/1.8V)	SMBus Data; Open Drain with pull-up on platform.
43	PETp0	PCIe TX Differential signal defined by the PCI Express M.2 spec
44	ALERT#(O) (0/1.8V)	Alert notification to master; Open Drain with pull-up on platform; Active low. NOTE : For pfail circuit designed in Host platform Normal – Pull high 1.8V Power loss – Drive low & FW receive interrupt and implement power loss flow
45	GND	Ground
46	N/C	No connect
47	PERn0	PCIe RX Differential signal defined by the PCI Express M.2 spec
48	N/C	No connect
49	PERp0	PCIe RX Differential signal defined by the PCI Express M.2 spec
50	PERST#(I)(0/3.3V)	PE-Reset is a functional reset to the card as defined by the PCIe Mini CEM specification.
51	GND	Ground
52	CLKREQ#(I/O)(0/3.3V)	Clock Request is a reference clock request signal as defined by the PCIe Mini CEM specification; Also used by L1 PM Sub-states.
53	REFCLKn	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
54	PEWAKE#(I/O)(0/3.3V)	PCIe PME Wake. Open Drain with pull up on platform; Active Low.
55	REFCLKp	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
56	Reserved for MFG DATA	Manufacturing Data line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
57	GND	Ground

Pin NO.	PCIe Pin	Description
58	Reserved for MFG CLOCK	Manufacturing Clock line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
59	Module Key M	Module Key
60	Module Key M	
61	Module Key M	
62	Module Key M	
63	Module Key M	
64	Module Key M	
65	Module Key M	
66	Module Key M	
67	N/C	No connect
68	SUSCLK(32KHz) (I)(0/3.3V)	32.768 kHz clock supply input that is provided by the platform chipset to reduce power and cost for the module.
69	N/C	PEDET (NC-PCIe)
70	3.3V	3.3V source
71	GND	Ground
72	3.3V	3.3V source
73	GND	Ground
74	3.3V	3.3V source
75	GND	Ground

7. NVMe Command List

■ Admin commands

Identifier	O/M	Command Description
00h	M	Delete I/O Submission Queue
01h	M	Create I/O Submission Queue
02h	M	Get Log Page
04h	M	Delete I/O Completion Queue
05h	M	Create I/O Completion Queue
06h	M	Identify
08h	M	Abort
09h	M	Set Feature
0Ah	M	Get Feature
0Ch	M	Asynchronous Event Request
10h	O	Firmware Commit
11h	O	Firmware Image Download
14h	O	Device Self-test
80h	O	Format NVM
81h	O	Security Send
82h	O	Security Receive
84h	O	Sanitize

■ NVM commands

Identifier	O/M	Command Description
00h	O	Flush
01h	O	Write
02h	O	Read
04h	O	Write Uncorrectable
05h	O	Compare
08h	O	Write Zeroes
09h	O	Dataset Management

■ Set Feature Commands

Identifier	O/M	Command Description
00h		Reserved
01h	M	Arbitration
02h	M	Power Management
03h	O	LBA Range Type
04h	M	Temperature Threshold
05h	M	Error Recovery
06h	O	Volatile Write Cache
07h	M	Number Of Queues
08h	M	Interrupt Coalescing
09h	M	Interrupt Vector Configuration
0Ah	M	Write Atomicity Normal
0Bh	M	Asynchronous Event Configuration
0Ch	O	Autonomous Power State Transition
0Dh	O	Host Memory Buffer
0Eh	O	Timestamp

Specifications subject to change without notice, contact your sales representatives for the most update information.

10h	O	Host Controlled Thermal Management
11h	O	Non-Operational Power State Config
0Eh - 7Dh		Reserved
80h	O	Software Progress Marker

■ Get Log Page Commands

Identifier	O/M	Command Description
00h		Reserved
01h	M	Error Information
02h	M	SMART / Health Information
03h	M	Firmware Slot Information
04h	O	Changed Namespace List
06h	O	Device Self-test
09h - 7Fh		Reserved
81h	O	Sanitize Status
82h - FFh		Reserved

8. Identify Device Data

The Identify Device Data enables Host to receive parameter information from the device. The parameter words in the buffer have the arrangement and meanings defined in below table. All reserve bits or words are zero

■ Identify Controller Data Structure

Bytes	O/M	Description	Default Value
01:00	M	PCI Vendor ID (VID)	0x1987
03:02	M	PCI Subsystem Vendor ID (SSVID)	0x1987
23:04	M	Serial Number (SN)	TBD
63:24	M	Model Number (MN)	TBD
71:64	M	Firmware Revision (FR)	TBD
72	M	Recommended Arbitration Burst (RAB)	0x01
75:73	M		0x6479A7
76	O		0x00
77	M	Maximum Data Transfer Size (MDTS)	0x09
79:78	M	Controller ID (CNTLID)	0x0001
83:80	M	Version (VER)	0x00010300
87:84	M	RTD3 Resume Latency (RTD3R)	0x00989680 (10 Sec)
91:88	M	RTD3 Entry Latency (RTD3E)	0x00989680 (10 Sec)
95:92	M	IEEE OUI Identifier (IEEE)	0x00000200
99:96	M	Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC)	0x0002
111:100	O	Reserved	0x00
127:112	O	FRU Globally Unique Identifier (FGUID)	0x00
239:128	-	Reserved	0x00
255:240	-	Refer to the NVMe Management Interface Specification for definition	0x00
257:256	M	Optional Admin Command Support (OACS)	0x0017
258	M	Abort Command Limit (ACL)	0x03
259	M	Asynchronous Event Request Limit (AERL)	0x03
260	M	Firmware Updates (FRMW)	0x12
261	M	Log Page Attributes (LPA)	0x8
262	M	Error Log Page Entries (ELPE)	0x3E
263	M	Number of Power States Support (NPSS)	0x0
264	M	Admin Vendor Specific Command Configuration (AVSCC)	0x01
265	O	Autonomous Power State Transition Attributes (APSTA)	0x0
267:266	M	Warning Composite Temperature Threshold (WCTEMP)	0x016B
269:268	M	Critical Composite Temperature Threshold (CCTEMP)	0x170
271:270	O	Maximum Time for Firmware Activation (MTFA)	0x64 10sec
275:272	O	Host Memory Buffer Preferred Size (HMPRE)	0x00000000
279:276	O	Host Memory Buffer Minimum Size (HMMIN)	0x00000000
295:280	O	Total NVM Capacity (TNVMCAP)	**
311:296	O	Unallocated NVM Capacity (UNVMCAP)	**
315:312	O	Replay Protected Memory Block Support (RPMBS)	0x00000000
317:316	O	Extended Device Self-test Time (EDSTT)	0x0A
318	O	Device Self-test Options (DSTO)	0x0
319	M	Firmware Update Granularity (FWUG)	0x01
321:320	M	Keep Alive Support (KAS)	0x0000
323:322	O	Host Controlled Thermal Management Attributes (HCTMA)	0x01
325:324	O	Minimum Thermal Management Temperature (MNTMT)	0x139
327:326	O	Maximum Thermal Management Temperature (MXTMT)	0x166
331:328	O	Sanitize Capabilities (SANICAP)	0x00000000
511:332	-	Reserved	0x00

NVM Command Set Attributes			
512	M	Submission Queue Entry Size (SQES)	0x66
513	M	Completion Queue Entry Size (CQES)	0x44
515:514	M	Maximum Outstanding Commands (MAXCMD)	0x100
519:516	M	Number of Namespaces (NN)	0x00000001
521:520	M	Optional NVM Command Support (ONCS)	0x5D
523:522	M	Fused Operation Support (FUSES)	0x0000
524	M	Format NVM Attributes (FNA)	0x00
525	M	Volatile Write Cache (VWC)	0x01
527:526	M	Atomic Write Unit Normal (AWUN)	TBD
529:528	M	Atomic Write Unit Power Fail (AWUPF)	TBD
530	M	NVM Vendor Specific Command Configuration (NVSCC)	0x01
531	M	Reserved	0x00
533:532	O	Atomic Compare & Write Unit (ACWU)	0x0000
535:534	M	Reserved	0x0000
539:536	O	SGL Support (SGLS)	0x00000000
767:540	M	Reserved	0x00
IO Command Set Attributes			
1023:768	M	NVM Subsystem NVMe Qualified Name (SUBNQN)	0x00
1791:1024	-	Reserved	0x00
2047:1792	-	Reserved	0x00
2079:2048	M	Power State 0 Descriptor (PSD0)	
2111:2080	O	Power State 1 Descriptor (PSD1)	0x00
2143:2112	O	Power State 2 Descriptor (PSD2)	0x00
2175:2144	O	Power State 3 Descriptor (PSD3)	0x00
2207:2176	O	Power State 4 Descriptor (PSD4)	0x00
2239:2208	O	Power State 5 Descriptor (PSD5)	0x00
2271:2240	O	Power State 6 Descriptor (PSD6)	0x00
2303:2272	O	Power State 7 Descriptor (PSD7)	0x00
2335:2304	O	Power State 8 Descriptor (PSD8)	0x00
2367:2336	O	Power State 9 Descriptor (PSD9)	0x00
2399:2368	O	Power State 10 Descriptor (PSD10)	0x00
2431:2400	O	Power State 11 Descriptor (PSD11)	0x00
2463:2432	O	Power State 12 Descriptor (PSD12)	0x00
2495:2464	O	Power State 13 Descriptor (PSD13)	0x00
2527:2496	O	Power State 14 Descriptor (PSD14)	0x00
2559:2528	O	Power State 15 Descriptor (PSD15)	0x00
2591:2560	O	Power State 16 Descriptor (PSD16)	0x00
2623:2592	O	Power State 17 Descriptor (PSD17)	0x00
2655:2624	O	Power State 18 Descriptor (PSD18)	0x00
2687:2656	O	Power State 19 Descriptor (PSD19)	0x00
2719:2688	O	Power State 20 Descriptor (PSD20)	0x00
2751:2720	O	Power State 21 Descriptor (PSD21)	0x00
2783:2752	O	Power State 22 Descriptor (PSD22)	0x00
2815:2784	O	Power State 23 Descriptor (PSD23)	0x00
2847:2816	O	Power State 24 Descriptor (PSD24)	0x00
2879:2848	O	Power State 25 Descriptor (PSD25)	0x00
2911:2880	O	Power State 26 Descriptor (PSD26)	0x00
2943:2912	O	Power State 27 Descriptor (PSD27)	0x00
2975:2944	O	Power State 28 Descriptor (PSD28)	0x00
3007:2976	O	Power State 29 Descriptor (PSD29)	0x00
3039:3008	O	Power State 30 Descriptor (PSD30)	0x00
3071:3040	O	Power State 31 Descriptor (PSD31)	0x00

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Vendor Specific			
3278:3072	O	Vendor Specific (VS)	0x00
3279	O	Vendor Specific (VS)	0x0
4095:3072	O	Vendor Specific (VS)	Reserved

* The OUI shall be a valid IEEE/RAC assigned identifier that may be registered at <http://standards.ieee.org/develop/regauth/oui/public.html>.

** depends on the using of capacity

Identify Namespace Data Structure & NVM Command Set Specific

Bytes	O/M	Description	Default Value
7:0	M	Namespace Size (NSZE)	TBD*
15:8	M	Namespace Capacity (NCAP)	TBD*
23:16	M	Namespace Utilization (NUSE)	TBD*
24	M	Namespace Features (NSFEAT)	0x00
25	M	Number of LBA Formats (NLBAF)	0x01
26	M	Formatted LBA Size (FLBAS)	0x00
27	M	Metadata Capabilities (MC)	0x00
28	M	End-to-end Data Protection Capabilities (DPC)	0x00
29	M	End-to-end Data Protection Type Settings (DPS)	0x00
30	O	Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC)	0x00
31	O	Reservation Capabilities (RESCAP)	0x00
32	O	Format Progress Indicator (FPI)	0x00
33		Reserved	0x09
35:34	O	Namespace Atomic Write Unit Normal (NAWUN)	0x0000
37:36	O	Namespace Atomic Write Unit Power Fail (NAWUPF)	0x0000
39:38	O	Namespace Atomic Compare & Write Unit (NACWU)	0x0000
41:40	O	Namespace Atomic Boundary Size Normal (NABSN)	0x0000
43:42	O	Namespace Atomic Boundary Offset (NABO)	0x0000
45:44	O	Namespace Atomic Boundary Size Power Fail (NABSPF)	0x0000
47:46		Reserved	0x0000
63:48	O	NVM Capacity (NVMCAP)	0x00
103:64		Reserved	0x00
119:104	O	Namespace Globally Unique Identifier (NGUID)	0x0
127:120	O	IEEE Extended Unique Identifier (EUI64)	0x373900F0FFA77964
131:128	M	LBA Format 0 Support (LBAF0)	0x02090000
135:132	O	LBA Format 1 Support (LBAF1)	0x00000000
139:136	O	LBA Format 2 Support (LBAF2)	0x00000000
143:140	O	LBA Format 3 Support (LBAF3)	0x00000000
147:144	O	LBA Format 4 Support (LBAF4)	0x00000000
151:148	O	LBA Format 5 Support (LBAF5)	0x00000000
155:152	O	LBA Format 6 Support (LBAF6)	0x00000000
159:156	O	LBA Format 7 Support (LBAF7)	0x00000000
163:160	O	LBA Format 8 Support (LBAF8)	0x00000000
167:164	O	LBA Format 9 Support (LBAF9)	0x00000000
171:168	O	LBA Format 10 Support (LBAF10)	0x00000000
175:172	O	LBA Format 11 Support (LBAF11)	0x00000000
179:176	O	LBA Format 12 Support (LBAF12)	0x00000000
183:180	O	LBA Format 13 Support (LBAF13)	0x00000000
187:184	O	LBA Format 14 Support (LBAF14)	0x00000000
191:188	O	LBA Format 15 Support (LBAF15)	0x00000000
383:192		Reserved	0x00

*See IDEMA SPEC

** See IEEE EUI-64 SPEC

Specifications subject to change without notice, contact your sales representatives for the most update information.

■ List of Device Identification for Each Capacity

Capacity (GB)	Byte[7:0]: Namespace Size (NSZE)	Byte[7:0]: Namespace Size (NSZE) (Dec)
480	37E436B0h	937,703,088
960	6FC81AB0h	1,875,385,008
1920	DF8FE2B0h	3,750,748,848
3840	1BF1F72B0	7,501,476,528

9. SMART Attributes

ID	ATTRIBUTE_NAME	Log Identifier	# of Bytes	Byte index	Unit
01h	Critical Warning	02h	1	[0]	-
02h	Composite Temperature	02h	2	[2:1]	°K
03h	Available Spare	02h	1	[3]	%
04h	Available Spare Threshold	02h	1	[4]	%
05h	Percentage Used	02h	1	[5]	%
06h-10h	Reserved	02h		[31:6]	
11h	Data Units Read	02h	16	[47:32]	1000 Sectors
12h	Data Units Written (Host Write)	02h	16	[63:48]	1000 Sectors
13h	Host Read Commands	02h	16	[79:64]	count
14h	Host Write Commands	02h	16	[95:80]	count
15h	Controller Busy Time	02h	16	[111:96]	mins
16h	Power Cycles	02h	16	[127:112]	count
17h	Power on Hours	02h	16	[143:128]	hours
18h	Unsafe Shutdowns	02h	16	[159:144]	count
19h	Media and Data Integrity Errors	02h	16	[175:160]	times
1Ah	Number of Error Information Log Entries	02h	16	[191:176]	count
1Bh	Warning Composite Temperature Time	02h	4	[195:192]	mins
1Ch	Critical Composite Temperature Time	02h	4	[199:196]	mins
1Dh	Temperature Sensor 1	02h	2	[201:200]	°K
1Eh	Temperature Sensor 2	02h	2	[203:202]	°K
1Fh	Temperature Sensor 3	02h	2	[205:204]	°K
20h	Temperature Sensor 4	02h	2	[207:206]	°K
21h	Temperature Sensor 5	02h	2	[209:208]	°K
22h	Temperature Sensor 6	02h	2	[211:210]	°K
23h	Temperature Sensor 7	02h	2	[213:212]	°K
24h	Temperature Sensor 8	02h	2	[215:214]	°K
25h	Thermal Management Temperature 1 Transition Count	02h	4	[219:216]	count
26h	Thermal Management Temperature 2 Transition Count	02h	4	[223:220]	count
27h	Total Time for Thermal Management Temperature 1:	02h	4	[227:224]	Second

28h	Total Time for Thermal Management Temperature 2:	02h	4	[231:228]	Second
29h-4Fh	Reserved	02h		[511:232]	

10. System Power Consumption

■ Supply Voltage

Parameter	Rating
Operating Voltage	3.3V

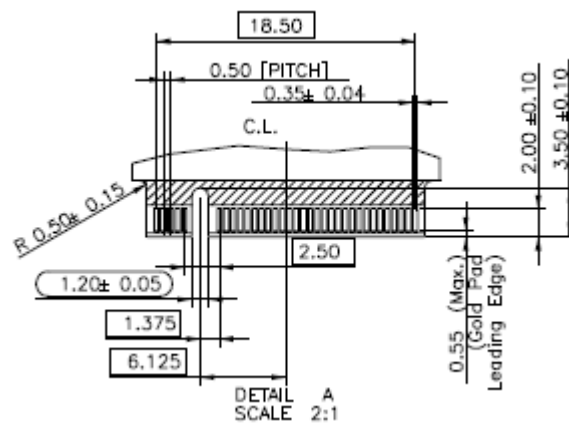
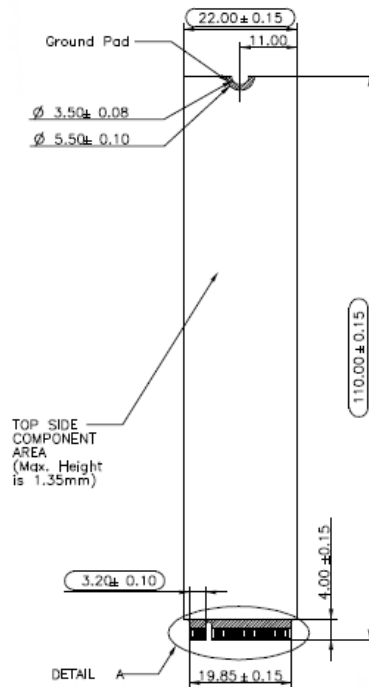
■ Power Consumption

(W)		Read	Write
3D TLC	480 GB	7.0	5.2
	960 GB	7.2	6.1
	1920 GB	7.2	7.1
	3840 GB	8.1	7.3

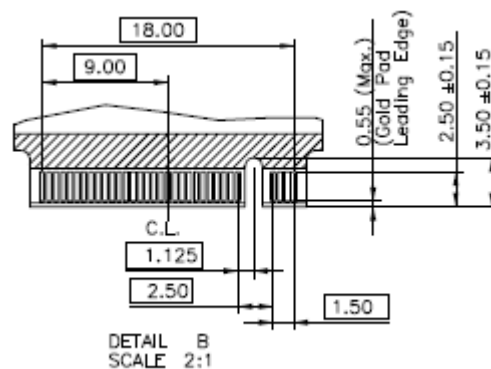
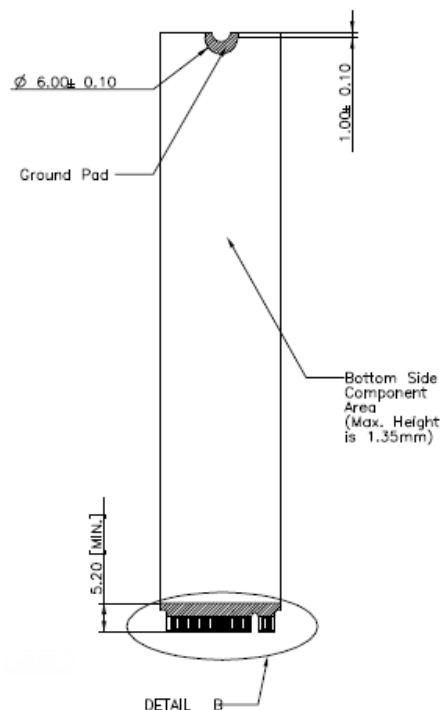
Notes:

1. From Oct 2019, Toshiba Memory officially changed company's name to Kioxia
2. Use CrystalDiskMark 6.0 with the setting of 1000MB. Sequentially read and write the disk for 5 times, and measure power consumption during sequential Read [1/5]~[5/5] or sequential Write [1/5]~[5/5]
3. Power Consumption may differ according to flash configuration and platform.
4. The measured power voltage is 3.3V.

11. Physical Dimension M.2 22110 PCIe SSD (Unit: mm)



Top View



Bottom View

Appendix: Part Number Table

Product	Advantech PN
SQF 920 NVMe M.2 22110 SSD (OPAL) 480G 3D TLC (0~70°C)	SQF-CMBV8-480G-ECC
SQF 920 NVMe M.2 22110 SSD (OPAL) 960G 3D TLC (0~70°C)	SQF-CMBV8-960G-ECC
SQF 920 NVMe M.2 22110 SSD (OPAL) 1920G 3D TLC (0~70°C)	SQF-CMBV8-1K9G-ECC
SQF 920 NVMe M.2 22110 SSD (OPAL) 3840G 3D TLC (0~70°C)	SQF-CMBV8-3K8G-ECC
SQF 920 NVMe M.2 22110 SSD (OPAL) 480G 3D TLC (-40~85°C)	SQF-CMBV8-480G-ECE
SQF 920 NVMe M.2 22110 SSD (OPAL) 960G 3D TLC (-40~85°C)	SQF-CMBV8-960G-ECE
SQF 920 NVMe M.2 22110 SSD (OPAL) 1920G 3D TLC (-40~85°C)	SQF-CMBV8-1K9G-ECE
SQF 920 NVMe M.2 22110 SSD (OPAL) 3840G 3D TLC (-40~85°C)	SQF-CMBV8-3K8G-ECE