CXL 2.0 Memory E3.S 2T Type 3 64GB Datasheet

(SQR-CX5N64G52B)

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Revision History

Rev	Date	Modification
1.0	1st Aug, 2024	Official release

1. Description

Part Number	Density	Interface Speed	IC Configuration	Organization	Number of DRAM	Number of rank	side	ECC
SQR-CX5N64G52B	64GB	PCIe Gen 5.x8	2Gx8(16Gb)	8Gx80	40	2	2	Y

2. Features

- Compliant with PCI Express® Base Specification Rev. 5.0
- Compliant with CXL™ 1.1 & CXL™ 2.0
- PCIe / CXL io Base
  - ◆ Single link with x8 lanes
  - ◆ Up to 32GT data rate
- Type -3 Single Logical Device
- Support SFF-TA-1002 & 1009 SMBus
- RoHS/Halogen-free
- Temperature – Operating: 0~70°C
- Supply Voltage / Tolerance: 12V±10%
- Power Consumption – Active Power: 39.1W
- Width: 76.00±0.25mm
- Length: 112.75±0.4mm
- Height: 16.8+0/-0.3mm
- Weight: Up to 245 g
- Led Information:

  -Green Color (Driven by the device)

  -Amber / Blue Color (Driven by the host)

3. LED Information

◆ The usage and details of the LEDs on EDSFF devices follows SNIA SFF-TA-1009 Rev3.1

LED description	Green	Amber	Blue
Driven by	Device	Host (LED signal)	Host (LED signal)
Function	Power, Activity	Host Defined	Host Defined

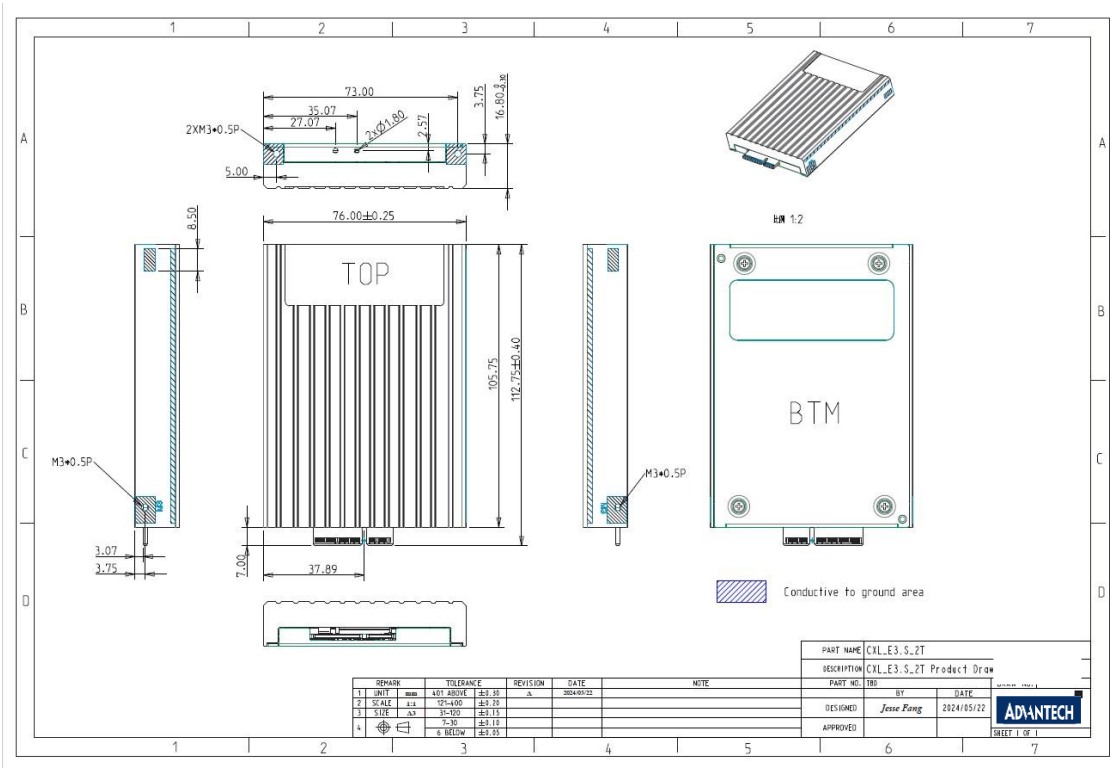
-Green Color (Driven by the device)

-Amber / Blue Color (Driven by the host)

4. Dimension

- EDSFF E3.S 2T Physical

Parameter	Unit	Description
Width	mm	76.00±0.25
Length	mm	112.75±0.40
Height	mm	Max 16.8(16.8+0/-0.3)
Weight	g	Up to 245



5. Pin Descriptions

Pin	Contact Sequence	Signal	Signal	Contact Sequence	Pin
B1	2nd mate	12 V	GND	1st mate	A1
B2	2nd mate	12 V	GND	1st mate	A2
B3	2nd mate	12 V	GND	1st mate	A3
B4	2nd mate	12 V	GND	1st mate	A4
B5	2nd mate	12 V	GND	1st mate	A5
B6	2nd mate	12 V	GND	1st mate	A6
B7	2nd mate	MFG	SMBCLK	2nd mate	A7
B8	2nd mate	RFU	SMBDATA	2nd mate	A8
B9	2nd mate	DUALPORTEN#	SMRST#	2nd mate	A9
B10	2nd mate	PERST0#	LED	2nd mate	A10
B11	2nd mate	3.3 Vaux	PERST1#	2nd mate	A11
B12	2nd mate	PWRDIS	PRSNT0#	2nd mate	A12
B13	1st mate	GND	GND	1st mate	A13
B14	2nd mate	REFCLKn0	REFCLKn1	2nd mate	A14
B15	2nd mate	REFCLKp0	REFCLKp1	2nd mate	A15
B16	1st mate	GND	GND	1st mate	A16
B17	2nd mate	PETn0	PERn0	2nd mate	A17
B18	2nd mate	PETp0	PERp0	2nd mate	A18
B19	1st mate	GND	GND	1st mate	A19
B20	2nd mate	PETn1	PERn1	2nd mate	A20
B21	2nd mate	PETp1	PERp1	2nd mate	A21
B22	1st mate	GND	GND	1st mate	A22
B23	2nd mate	PETn2	PERn2	2nd mate	A23
B24	2nd mate	PETp2	PERp2	2nd mate	A24
B25	1st mate	GND	GND	1st mate	A25
B26	2nd mate	PETn3	PERn3	2nd	A26

				mate	
B27	2nd mate	PETp3	PERp3	2nd mate	A27
B28	1st mate	GND	GND	1st mate	A28
		Key	Key		
B29	1st mate	GND	GND	1st mate	A29
B30	2nd mate	PETn4	PERn4	2nd mate	A30
B31	2nd mate	PETp4	PERp4	2nd mate	A31

6. SPD

Byte Number	Function Described	Function supported	Hex Value
0	Number of Bytes in SPD Device	1024 Bytes	30
1	SPD Revision for Base Configuration Parameters	Revision 1.0	10
2	Key Byte / Host Bus Command Protocol Type	DDR5 SDRAM	12
3	Key Byte / Module Type	RDIMM	01
4	First SDRAM Density and Package	Monolithic 16Gb	04
5	First SDRAM Addressing	10 columns/16 rows	00
6	First SDRAM I/O Width	x8	20
7	First SDRAM Bank Groups & Banks Per Bank Group	8BGs / 4Banks per BG	62
8	Second SDRAM Density and Package	N/A	00
9	Second SDRAM Addressing	N/A	00
10	Second SDRAM I/O Width	N/A	00
11	Second SDRAM Bank Groups & Banks Per Bank Group	N/A	00
12	SDRAM BL32 & Post Package Repair	BL32 supported / sPPR	B0
13	SDRAM Duty Cycle Adjuster & Partial Array Self Refresh	PASR not supported	02
14	SDRAM Fault Handling	Yes	01
15	Reserved	Reserved	00
16	SDRAM Nominal Voltage, VDD	1.1V	00
17	SDRAM Nominal Voltage, VDDQ	1.1V	00
18	SDRAM Nominal Voltage, VPP	1.8V	00
19	SDRAM Timing	Standard	00
20	SDRAM Minimum Cycle Time (t_{CKAVG}min), Least Significant Byte	357ps	65
21	SDRAM Minimum Cycle Time (t_{CKAVG}min), Most Significant Byte	357ps	01
22	SDRAM Maximum Cycle Time (t_{CKAVG}max), Least Significant Byte	1010ps	F2
23	SDRAM Maximum Cycle Time (t_{CKAVG}max), Most Significant Byte	1010ps	03
24	CAS Latencies Supported, First Byte	22,26,28,30,32,36,40,42,46,50	7A
25	CAS Latencies Supported, Second Byte	22,26,28,30,32,36,40,42,46,50	AD
26	CAS Latencies Supported, Third Byte	22,26,28,30,32,36,40,42,46,50	00
27	CAS Latencies Supported, Fourth Byte	22,26,28,30,32,36,40,42,46,50	00
28	CAS Latencies Supported, Fifth Byte	22,26,28,30,32,36,40,42,46,50	00
29	Reserved	Reserved	00
30	SDRAM Minimum CAS Latency Time (t_{AA}min), Least Significant Byte	16000ps	80
31	SDRAM Minimum CAS Latency Time (t_{AA}min), Most Significant Byte	16000ps	3E
32	SDRAM Minimum RAS to CAS Delay Time (t_{RCD}min), Least Significant Byte	16000ps	80
33	SDRAM Minimum RAS to CAS Delay Time (t_{RCD}min), Most Significant Byte	16000ps	3E
34	SDRAM Minimum Row Precharge Delay Time (t_{RP}min), Least Significant Byte	16000ps	80
35	SDRAM Minimum Row Precharge Delay Time (t_{RP}min), Most Significant Byte	16000ps	3E
36	SDRAM Minimum Active to Precharge Delay Time (t_{RAS}min), Least Significant Byte	32000ps	00
37	SDRAM Minimum Active to Precharge Delay Time (t_{RAS}min), Most Significant Byte	32000ps	7D

38	SDRAM Minimum Active to Active/Refresh Delay Time (t_{RC}min), Least Significant Byte	48000os	80
39	SDRAM Minimum Active to Active/Refresh Delay Time (t_{RC}min), Most Significant Byte	48000os	BB
40	SDRAM Minimum Write Recovery Time (t_{WR}min), Least Significant Byte	30000ps	30
41	SDRAM Minimum Write Recovery Time (t_{WR}min), Most Significant Byte	30000ps	75
42	SDRAM Minimum Refresh Recovery Delay Time (t_{RFC1}min, t_{RFC1}_slr min), Least Significant Byte	295ns	27
43	SDRAM Minimum Refresh Recovery Delay Time (t_{RFC1}min, t_{RFC1}_slr min), Most Significant Byte	295ns	01
44	SDRAM Minimum Refresh Recovery Delay Time (t_{RFC2}min, t_{RFC2}_slr min), Least Significant Byte	160ns	A0
45	SDRAM Minimum Refresh Recovery Delay Time (t_{RFC2}min, t_{RFC2}_slr min), Most Significant Byte	160ns	00
46	SDRAM Minimum Refresh Recovery Delay Time (t_{RFCsb}min, t_{RFCsb}_slr min), Least Significant Byte	130ns	82
47	SDRAM Minimum Refresh Recovery Delay Time (t_{RFCsb}_dlr min), Most Significant Byte	130ns	00
48	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFC1}_dlr min), Least Significant Byte	N/A	00
49	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFC1}_dlr min), Most Significant Byte	N/A	00
50	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFC2}_dlr min), Least Significant Byte	N/A	00
51	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFC2}_dlr min), Most Significant Byte	N/A	00
52	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFCsb}_dlr min), Least Significant Byte	N/A	00
53	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFCsb}_dlr min), Most Significant Byte	N/A	00
54	SDRAM Refresh Management, First Byte, First SDRAM	N/A	00
55	SDRAM Refresh Management, Second Byte, First SDRAM	N/A	00
56	SDRAM Refresh Management, First Byte, Second SDRAM	N/A	00
57	SDRAM Refresh Management, Second Byte, Second SDRAM	N/A	00
58	SDRAM Adaptive Refresh Management Level A, First Byte, First SDRAM	N/A	00
59	SDRAM Adaptive Refresh Management Level A, Second Byte, First SDRAM	N/A	00
60	SDRAM Adaptive Refresh Management Level A, First Byte, Second SDRAM	N/A	00
61	SDRAM Adaptive Refresh Management Level A, Second Byte, Second SDRAM	N/A	00
62	SDRAM Adaptive Refresh Management Level B, First Byte, First SDRAM	N/A	00
63	SDRAM Adaptive Refresh Management Level B, Second Byte, First SDRAM	N/A	00
64	SDRAM Adaptive Refresh Management Level B, First Byte, Second SDRAM	N/A	00
65	SDRAM Adaptive Refresh Management Level B, Second Byte, Second SDRAM	N/A	00
66	SDRAM Adaptive Refresh Management Level C, First Byte, First SDRAM	N/A	00
67	SDRAM Adaptive Refresh Management Level C, Second Byte, First SDRAM	N/A	00
68	SDRAM Adaptive Refresh Management Level C, First Byte, Second SDRAM	N/A	00
69	SDRAM Adaptive Refresh Management Level C, Second Byte, Second SDRAM	N/A	00
70	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group (t_{RRD_L}min), Least Significant Byte	5000ps	88
71	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group (t_{RRD_L}min), Most Significant Byte	5000ps	13
72	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group (t_{RRD_L}min), Lower Clock Limit	8nCK	08
73	SDRAM Minimum CAS_n to CAS_n Command Delay Time, Same Bank Group (tCCD_Lmin), Least Significant Byte	5000ps	88

74	SDRAM Minimum CAS_n to CAS_n Command Delay Time, Same Bank Group (tCCD_Lmin), Most Significant Byte	5000ps	13
75	SDRAM Minimum CAS_n to CAS_n Command Delay Time, Same Bank Group (tCCD_Lmin), Lower Clock Limit	8nCK	08
76	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group ($t_{CCD_L_WR}$min), Least Significant Byte	20000ps	20
77	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group ($t_{CCD_L_WR}$min), Most Significant Byte	20000ps	4E
78	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group ($t_{CCD_L_WR}$min), Lower Clock Limit	32nCK	20
79	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Second Write not RMW, Same Bank Group ($t_{CCD_L_WR2}$min), Least Significant Byte	10000ps	10
80	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Second Write not RMW, Same Bank Group ($t_{CCD_L_WR2}$min), Most Significant Byte	10000ps	27
81	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Second Write not RMW, Same Bank Group ($t_{CCD_L_WR2}$min), Lower Clock Limit	16nCK	10
82	SDRAM Minimum Four Activate Window (t_{FAW}min), Least Significant Byte	11428ps	A4
83	SDRAM Minimum Four Activate Window (t_{FAW}min), Most Significant Byte	11428ps	2C
84	SDRAM Minimum Four Activate Window (t_{FAW}min), Lower Clock Limit	32nCK	20
85	SDRAM Minimum Internal Write to Read Command Delay Time, Same Bank Group, (t_{WTR_L}min), Least Significant Byte	10000ps	10
86	SDRAM Minimum Internal Write to Read Command Delay Time, Same Bank Group, (t_{WTR_L}min), Most Significant Byte	10000ps	27
87	SDRAM Minimum Internal Write to Read Command Delay Time, Same Bank Group, (t_{WTR_L}min), Lower Clock Limit	16nCK	10
88	SDRAM Minimum Internal Write to Read Command Delay Time, Different Bank Group, (t_{WTR_S}min), Least Significant Byte	2500ps	C4
89	SDRAM Minimum Internal Write to Read Command Delay Time, Different Bank Group, (t_{WTR_S}min), Most Significant Byte	2500ps	09
90	SDRAM Minimum Internal Write to Read Command Delay Time, Different Bank Group, (t_{WTR_S}min), Lower Clock Limit	4nCK	04
91	SDRAM Minimum Internal Read to Precharge Command Delay Time, (t_{RTP}min), Least Significant Byte	7500ps	4C
92	SDRAM Minimum Internal Read to Precharge Command Delay Time, (t_{RTP}min), Most Significant Byte	7500ps	1D
93	SDRAM Minimum Internal Read to Precharge Command Delay Time, (t_{RTP}min), Lower Clock Limit	12nCK	0C
94~127	Reserved -- must be coded as 0x00	Reserved	00
128~191	Reserved for future use	Reserved	00
192	SPD Revision for SPD bytes 192~447	Revision 1.0	10
193	Hashing Sequence	No authentication	00
194	SPD Manufacturer ID Code, First Byte	Renesas	80
195	SPD Manufacturer ID Code, Second Byte	Renesas	B3
196	SPD Device Type	Renesas	80
197	SPD Device Revision Number	Renesas	21
198	PMIC 0 Manufacturer ID Code, First Byte	Montage	86
199	PMIC 0 Manufacturer ID Code, Second Byte	Montage	32
200	PMIC 0 Device Type	Montage	80
201	PMIC 0 Revision Number	Montage	14
202	PMIC 1 Manufacturer ID Code, First Byte	N/A	00
203	PMIC 1 Manufacturer ID Code, Second Byte	N/A	00
204	PMIC 1 Device Type	N/A	00

205	PMIC 1 Revision Number	N/A	00
206	PMIC 2 Manufacturer ID Code, First Byte	N/A	00
207	PMIC 2 Manufacturer ID Code, Second Byte	N/A	00
208	PMIC 2 Device Type	N/A	00
209	PMIC 2 Revision Number	N/A	00
210	Thermal Sensor Manufacturer ID Code, First Byte	IDT (Renesas)	80
211	Thermal Sensor Manufacturer ID Code, Second Byte	IDT (Renesas)	B3
212	Thermal Sensor Device Type	IDT (Renesas)	C0
213	Thermal Sensor Revision Number	IDT (Renesas)	12
214	DRAM Specification Level	Reserved	00
215	SPD Specification Level	N/A	00
216	PMIC0 Specification Level	N/A	00
217	PMIC1 Specification Level	N/A	00
218	PMIC2 Specification Level	N/A	00
219	TS Specification Level	N/A	00
220	DIMM Specification Level	N/A	00
221~229	Reserved	Reserved	00
230	Module Nominal Height	31 < height <= 32 mm	11
231	Module Maximum Thickness	Back 2 < thickness <= 3 mm, front 1 < thickness <= 2 mm	21
232	Reference Raw Card Used	R/C E rev 0	04
233	DIMM Attributes	Tc 0 to +95 °C, 1row	81
234	Module Organization	Symmetrical 2 Package Ranks	08
235	Memory Channel Bus Width	2 channels, 32 bits per channel, 8 bits ECC	32
236~239	Reserved	Reserved	00
240	Registering Clock Driver Manufacturer ID Code, First Byte	Rambus	86
241	Registering Clock Driver Manufacturer ID Code, Second Byte	Rambus	9D
242	Register Device Type	Rambus	80
243	Register Revision Number	Rambus	10
246	Data Buffer Device Type	N/A	00
247	Data Buffer Revision Number	N/A	00
248	RCD-RW08 Clock Driver Enable	Enabled	00
249	RCD-RW09 Output Address and Control Enable	Enabled	00
250	RCD-RW0A QCK Driver Characteristics	Normal	2A
251	RCD-RW0B	Normal	4A
252	RCD-RW0C QxCA and QxCS_n Driver Characteristics	Normal	55
253	RCD-RW0D Data Buffer Interface Driver Characteristics	Normal	00
254	RCD-RW0E QCK, QCA and QCS Output Slew Rate	Normal	01
255	RCD-RW0F BCK, BCOM, and BCS Output Slew Rate	Normal	00
256	DB-RW86 DQS RTT Park Termination	Normal	00
257~447	Reserved	Reserved	00

448~509	Reserved for future use	Reserved	00
510~511	CRC for SPD bytes 0~509	CRC	B9 38
512	Module Manufacturer ID Code, First Byte	Advantech	8A
513	Module Manufacturer ID Code, Second Byte	Advantech	C8
514	Module Manufacturing Location	Made in Taiwan	02
515~516	Module Manufacturing Date		-
517~520	Module Serial Number		-
521~550	Module Part Number	SQR-CX5N64G52B	4D 4D 31 31 31 2D 35 43 47 53 31 41 31 41 43 41 30 30 20 20 20 20 20 20 20 20 20 20 20 20
551	Module Revision Code		00
552	DRAM Manufacturer ID Code, First Byte	Samsung	80
553	DRAM Manufacturer ID Code, Second Byte	Samsung	CE
554	DRAM Stepping		00
555~639	Manufacturer's Specific Data		-
640~703	End User Programmable	Reserved	00
704~767	End User Programmable	Reserved	00
768~831	End User Programmable	Reserved	00
832~895	End User Programmable	Reserved	00
896~959	End User Programmable	Reserved	00
960~1023	End User Programmable	Reserved	00

Appendix: Part Number Table

Product	Advantech PN
DDR5 CXL 2.0 E3.S-2T Type3 PCIE5.0 64GB (0-70C)	SQR-CX5N64G52B