產品承認書
(APPROVAL SHEET)

公司名稱 (Customer)： 研華股份有限公司

產品名稱 (Part Description)： SSD 固態硬碟

製造原廠 (Manufacture)： 建興儲存科技股份有限公司

建興儲存品名 (Model Name): CL4-4D256/ CL4-4D512 / CL4-4D1024

建興儲存料號及FW對照表：

SSSTC Model Name	**Advantech PN**	**Firmware version**
CL4-4D256	96FD42-P256-TS	1.00
CL4-4D512	96FD42-P512-TS	1.00
CL4-4D1024	96FD42-P1TB-TS	1.00

晶片廠牌 (Chip brand)： **SMI 2267XT + TSB BiCS5 cTLC**

Density:	256/512/1024 GB	**Interface:**	PCIE
From Factor:	M.2 2242	**Operating Voltage:**	3.3 V
Ambient Non-OP Temp:	-40~+85°C	**Ambient OP Temp:**	0~70°C
CUSTOMER APPROVAL BY			

SOLID STATE STORAGE TECHNOLOGY CORPORATION

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ENGINEERING SPECIFICATIONS

Product Name: CL4-4DXXX
M.2 PCIe Gen4 x 4 Lane SSD

Author: Twingo Tseng

Version	History	Date
1.0	First Release to Advantech	2022/06/01

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1 INTRODUCTION

1.1 Overview:

The CL4-4DXXX PCIe Gen4 x 4 Lane series Solid State Drive (SSD) delivers leading performance in an industry standard M.2 type 2242-S3-M form factor while simultaneously improving system responsiveness for applications over standard rotating drive media or hard disk drives. By combining leading NAND flash memory technology with our innovative high performance firmware, ***Solid State Storage Technology Corporation*** delivers a SSD for PCIe hard disk drive drop-in replacement with enhanced performance, reliability, ruggedness and power savings. Since there are no rotating platters, moving heads, fragile actuators, or unnecessary delays due to spin-up time or positional seek time that can slow down the storage subsystem, significant I/O and throughput performance improvement is achieved as compared to rotating media or hard disk drives. This document describes the specifications of the CL4-4DXXX PCIe Gen4 x 4 Lane series M.2 SSD in M.2 type 2242-S3-M form factors.

The CL4-4DXXX PCIe Gen4 x 4 Lane series M.2 SSD primarily targets M.2 based laptop PCs, highly rugged client devices, as well as thin and light mini/sub-notebooks. Key attributes include high performance, low power, increased system responsiveness, high reliability, and enhanced ruggedness as compared to standard hard drives. The CL4-4DXXX PCIe Gen4 x 4 Lane series M.2 SSD is available in M.2 type 2242-S3-M form factor that are electrically, mechanically, and software compatible with existing M.2 slots. Our flexible design allows interchangeability with existing hard drives based on the M.2 interface standard.

1.2 Product Specification

1.2.1. Form Factor: M.2 type 2242-S3-M SSD form factor

1.2.2. Capacity: available now

M.2 2242-S3-M 256/512/1024GB (CL4-4D256/512/1024)

Table 1 User Addressable Sectors

Unformatted capacity	Total user addressable sectors in LBA mode
256GB	500,118,192
512GB	1,000,215,216
1024GB	2,000,409,264

Notes:

1). 1GB=1,000,000,000 bytes and not all of the memory can be used for storage.

2). 1 Sector = 512 bytes

1.2.3. Flash:

Triple-Level Cell (TLC) component with Toggle-Mode

1.2.4. Band Performance

Table 2 Maximum Sustained Read and Write Bandwidth on Windows 10 platform

Capacity	Access Type	MB/s
256 GB	Sequential Read	3200
	Sequential Write	2100
512 GB	Sequential Read	3500
	Sequential Write	2100
1024 GB	Sequential Read	3700
	Sequential Write	2600

Notes:

1). Performance measured using Crystal Disk Mark 7.0.0, QD8 T1, 1GiB test size, 5 cycles.

2). PCIe link speed is Gen4 x 4.

3). Write cache enabled & 4K boundary data.

4). Test by secondary drive (data drive & clean state).

5). Performance based on internal testing on STRIX X570-F/AMD Ryzen 5 3600X 6-Core Windows 10; Performance may vary on different platforms, NVMe driver and OS.

1.2.5. Read and Write IOPS

Table 3 Random Read/Write Input/Output Operations per Second on Windows 10 platform

Capacity	Access Type	IOPS
256 GB	4K Read (IOPS)	400K
	4K Write (IOPS)	350K
512 GB	4K Read (IOPS)	400K
	4K Write (IOPS)	350K
1024 GB	4K Read (IOPS)	450K
	4K Write (IOPS)	400K

Notes:

1). Performance measured using Crystal Disk Mark 7.0.0, QD32 T16, 1GiB test size, 5 cycles.

2). PCIe link speed is Gen4 x 4.

3). Write cache enabled & 4K boundary data.

4). Test by secondary drive (data drive & clean state).

5). Performance based on internal testing on STRIX X570-F/AMD Ryzen 5 3600X 6-Core Windows 10; Performance may vary on different platforms, NVMe driver and OS.

1.2.6. Ready Time

Table 4 Power on to Ready time Specifications

Power-on Sequence	Typical POR	Sudden POR
Complete the I/O Command	500ms	10s

Notes:

1). Write cache enabled

2). Device measured using Drive Master

3). PCIe link speed is Gen4 x 4.

4). Test results may be different on different platform.

5).Typical POR assumes proper shutdown (Power removal preceded by host Shutdown Notification)

1.2.7. Compatibility

-- NVM Express Specification

-- PCI Express Base Specification

-- PCI Express M.2 Electromechanical Specification

-- Microsoft latest WHCK Certification

-- Support Legacy and UEFI BIOS

1.2.8. Supported Operating System and Chipset

--Operating System

Windows 7 x86, x64 / Windows 8 x86, x64 / Windows 10

Linux series, Red Hat 6.5, Fedora, SUSE, Ubuntu

Windows Server 2008, 2012

--Chipset:

※Please make sure the BIOS of the used mother board be updated to the latest version.

Table 5 Tested platform w/o issues

Manufacturer	Platform	Chipset	Manufacturer	Platform	Chipset
Echo 13	Alienware AW13R2	Intel Sunrise Point-LP	Precision	7440 AIO	Intel Sunrise Point Q170
Echo 15	Alienware AW15R2	Intel Sunrise Point HM170	Precision	3420 SFF	Intel Sunrise Point C236
Echo 17	Alienware AW17R3	Intel Sunrise Point HM170	Precision	3620MT	Intel Sunrise Point C236
XPS 13	9350	Intel Sunrise Point-LP	Optiplex	3040 MT	Intel Sunrise Point H110
Precision	5510	Intel Sunrise Point CM236	Optiplex	3240 AIO	Intel Sunrise Point H110
XPS 15	9550	Intel Sunrise Point HM170	ASUS	Z170 DELUXE	Intel Sunrise Point Z170
Inspiron 15	7568	Intel Sunrise Point-LP			
Optiplex	3040 MT	Intel Sunrise Point H110			
OptiPlex	3240 AIO	Intel Sunrise Point M110			
ProDesk	490 G3 MT	Intel Sunrise Point H170			
ProDesk	600 G2 DM	Intel Sunrise Point Q150			
Inspiron	5559	Intel Sunrise Point-LP			
Inspiron 11	3153	Intel Sunrise Point-LP			
Inspiron 13	7353	Intel Sunrise Point-LP			
Predator 15	G9-591	Intel Sunrise Point HM170			
MS	Surface Pro 4	Intel Sunrise Point-LP			
XPS Desktop	8900	Intel Sunrise Point Z170			
Alienware	X51 R3	Intel Sunrise Point Z170			
OptiPlex	7040 SFF	Intel Sunrise Point Q170			
OptiPlex	5040 SFF				

1.2.9. Certifications

Table 7 Device Certifications

Certification	Description
CE compliant	Indicates conformity with the essential health and safety requirements set out in European Directives Low voltage Directive and EMC Directive
UL certified	Underwriters Laboratories, Inc. Component Recognition UL60950-1
BSMI	Compliance to the Taiwan EMC standard “Limits and methods of Radio Disturbance Characteristics of Information Technology Equipment, CNS 13438 Class B”
Microsoft WHQL	Microsoft Windows Hardware Quality Labs
RoHS compliant	Restriction of Hazardous Substance Directive

1.2.10. PCIe M.2 interface Power Management

3.3V Input/ Max current (Peak) : 2.8A

1.2.11. Power Consumption

Table 8 Operating Voltage & Current

Description	Min	Max	Unit
Operating voltage for 3.3V (+/- 5%)	3.135	3.465	V

Table 9 Power Consumption

Capacity	Operation	Max (RMS T=5s)	Unit
256 GB	Start-up	8.25	W
	Read-Write	8.25	W
512GB	Start-up	8.25	W
	Read-Write	8.25	W
1024GB	Start-up	8.25	W
	Read-Write	8.25	W

1.2.12. Temperature

Table 10 Temperature Relative Specifications

Environment	Mode	Min	Max	Unit
Ambient Temperature	Operating	0	70	°C
	Non-operating	-40	85	°C
Humidity	Operation	5	95	%
	Non-operation	5	95	%

Note:

Measured without condensation

1.2.13. Reliability

Table 11 Reliability specifications

Parameter	Value
Mean Time between Failure (MTBF) [1]	> 1,500,000 hours
Power on/off cycle[2]	50,000 cycles

Notes:

1).MTBF is calculated based on a Part Stress Analysis. It assumes nominal voltage with all other parameters within specified range.

2). Power on/off cycles is defined as power being removed from the drive, and the restored. Most host systems remove power from the drive when entering suspend and hibernate as well as on a system shutdown.

1.2.14 Endurance

Capacity	TBW (Total Bytes Written)
256GB	Up to 340 TB
512GB	Up to 680 TB
1024GB	Up to 1360 TB

Note: TBW value is derived from JEDEC based on population of SSDs statistics.

1.2.15. Shock and Vibration

Table 12 Shock and Vibration

Item	Mode	Timing/Frequency	Max
Shock[1]	Non-operating	At 0.5 msec half-sine	1500G
Vibration[2]	Non-operation	2-500 Hz	3.1 Grms

Notes:

1).Shock specifications assume that the SSD is mounted securely with the input vibration applied to the drive mounting screws. Stimulus may be applied in the X, Y or Z axis.

2).Vibration specifications assume that the SSD is mounted securely with the input vibration applied to the drive mounting screws. Stimulus may be applied in the X, Y or Z axis. The measured specification is in root mean squared form.

1.2.16. Electrostatic discharge (ESD)

Electromagnetic Immunity tests assume the SSD is properly installed in the representative host system. The drive operates properly without errors degradation in performance when subjected to radio frequency (RF) environments defined in the following table.

Table 13 Radio Frequency Specifications

Test	Description	Performance criteria	Reference standard
Electrostatic discharge	Contact ±4KV Air: ±8KV	A	IEC 61000-4-2:2008
Electrostatic discharge	Contact ±6KV Air: ±12KV	B	IEC 61000-4-2:2008
Electrostatic discharge	Contact ±8KV Air: ±15KV	C	IEC 61000-4-2:2008
Radiated RF immunity	80~1000MHz, 3V/m, 80% AM with 1 KHz sine 900 MHz, 3 V/m, 50% pulse modulation at 200Hz	A	IEC 61000-4-3:2008
Electrical fast transient	±1KV on AC mains ±0.5KV on external I/O	B	IEC 61000-4-4:2004 +Corr.1:2006 +Corr.2:2007
Surge immunity	±1KV differential ±2KV common, AC mains	B	IEC 61000-4-5:2005
Conducted RF immunity	150KHz~80 MHz, 3 Vrms, 80% AM with 1KHz sine	A	IEC 61000-4-6:2008
Power frequency magnetic field	50Hz, 1A/m (r.m.s.)	A	IEC 61000-4-6:2008

Notes:

1. Performance criterion A = The device shall continue to operate as intended, i.e., normal unit operation with no degradation of performance.
2. Performance criterion B = The device shall continue to operate as intended after completion of test, however, during the test, some degradation of performance is allowed as long as there is no data loss operator intervention to restore device function.
3. Performance criterion C = Temporary loss of function is allowed. Operator intervention is acceptable to restore device function.
4. Contact electrostatic discharge is applied to drive enclosure.

1.2.17. Weight:

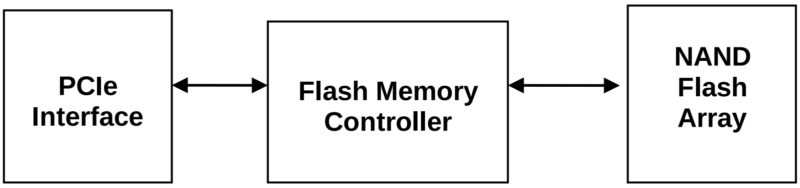
Weight spec. = 6 g Max.（CL4-4DXXX）

1.2.18. Dimension:

Form factor:

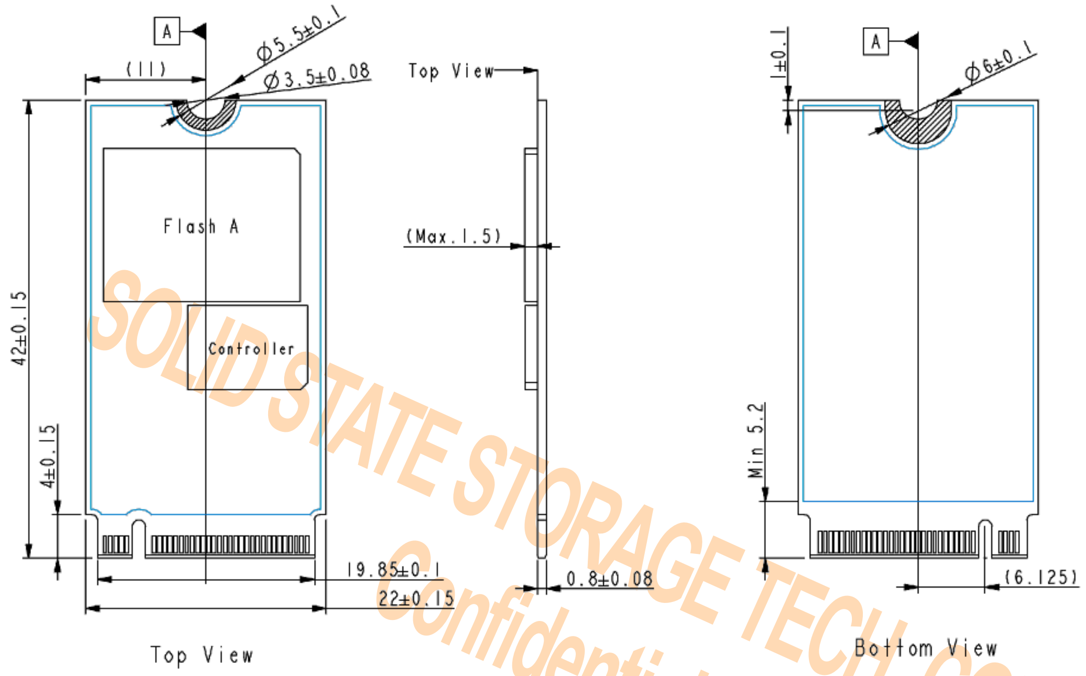
M.2 2242: 42.0 mm x 22.0 mm x 2.30 mm (L x W x H) （CL4-4DXXX）

1.3 Functional Block Diagram



1.4 Mechanical Drawing:

M.2 2242-S3-M: CL4-4DXXX



1.5 Architecture

The CL4-4DXXX PCIe Gen4 x 4 Lane Solid State Drive (SSD) utilizes a cost effective system-on-chip (SoC) design to provide a full 8GB/s bandwidth with the host while managing multiple flash memory devices on multiple channels internally.

1.6 Bootable Device:

The CL4-4DXXX PCIe Gen4 x 4 Lane Solid State Drive (SSD) is configured as a bootable device. This supported function allows users to manage it as a main system drive and to boot from PCIe SSD.

1.7 Power Mode Support

PCI Express feature enables the hardware to engage actively in automatic Link power management. CL4-3DXXX PCIe Gen4 x 4 Lane SSD Supports L0, L1, L1.1 and L1.2 mode.

-L0: Full On (Active power / Active mode) @PS0

-L1: Idle (Lower power / Idle mode) @PS0

-L1.2: Sleep (Lower power / Sleep mode) @PS4

The Link state transits automatically from L0 to L1, L1.1, or L1.2 state to save power when there is no data transferring. The device reduces power by gating internal clocks, and the CLKREQ# signal transited by host will enable lower power mode of some internal components such as PCIe PHY. Once the data can be transferred across the Link, the state will be brought back to L0 by the hardware.

Input Voltage	State			256 GB (W)	512 GB (W)	1024 GB (W)
3.3V ± 5%	PS0	Active Mode Max. Read/Write Performance (L0 state)	Rms	6	6	6
		Idle Mode (L1 state)		0.4	0.4	0.4
	PS3	Slumber Mode		0.05	0.05	0.05
	PS4	Sleep Mode (L1.2 state)		0.005	0.005	0.005

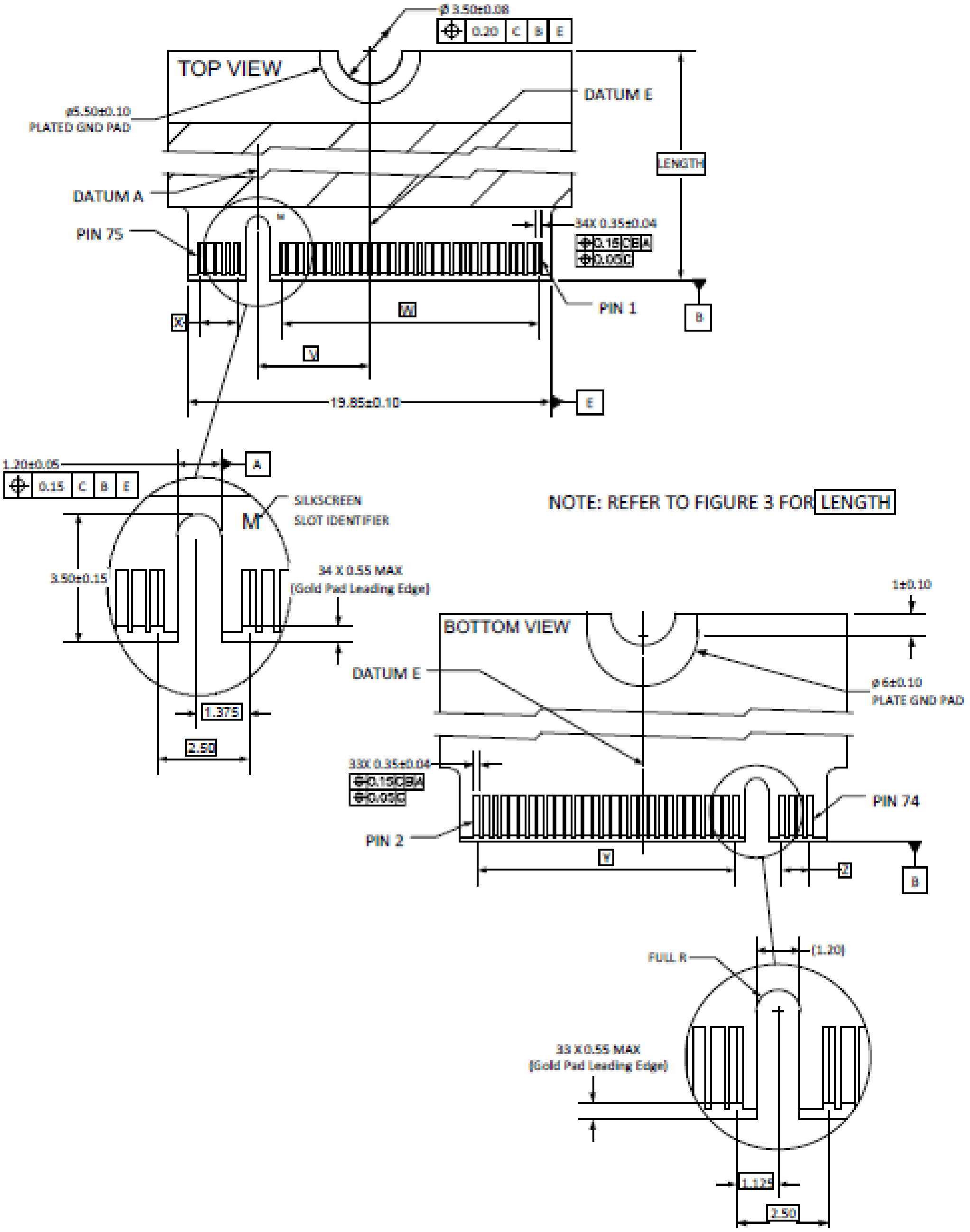
※L0 stands for power states after power-on and before entering L1,

※To enable L1 lower mode, the CLKREQ# signal must be sent by host.

2 PIN LOCATIONS AND SIGNAL DESCRIPTIONS

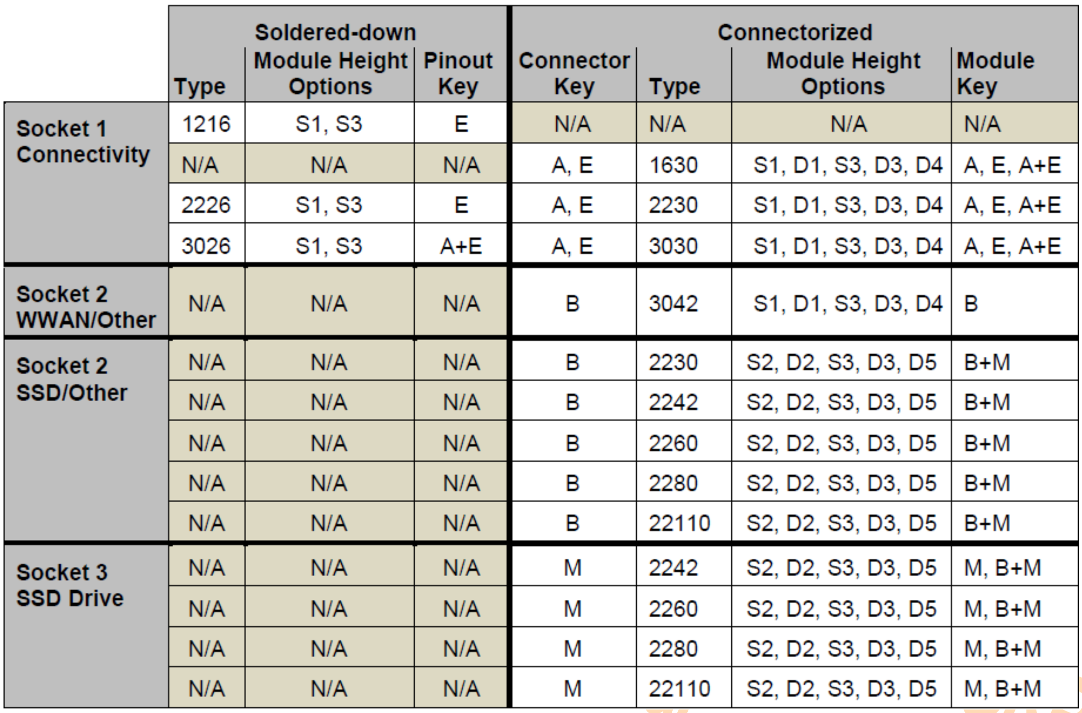
2.1 Pin Locations

The data and power connector pin locations of the CL4-3DXXX PCIe SSD Gen4 x 4 Lane are shown below. This M.2 device contains Socket 3 + M key.



2.2 M.2 Socket Definition

The PCI Express interface supported in Socket 3 is a 4 Lane PCI Express interface intended for premium SSD devices that need this sort of host interface.



	Soldered-down			Connectorized			
	Type	Module Height Options	Pinout Key	Connector Key	Type	Module Height Options	Module Key
Socket 1 Connectivity	1216	S1, S3	E	N/A	N/A	N/A	N/A
	N/A	N/A	N/A	A, E	1630	S1, D1, S3, D3, D4	A, E, A+E
	2226	S1, S3	E	A, E	2230	S1, D1, S3, D3, D4	A, E, A+E
	3026	S1, S3	A+E	A, E	3030	S1, D1, S3, D3, D4	A, E, A+E
Socket 2 WWAN/Other	N/A	N/A	N/A	B	3042	S1, D1, S3, D3, D4	B
Socket 2 SSD/Other	N/A	N/A	N/A	B	2230	S2, D2, S3, D3, D5	B+M
	N/A	N/A	N/A	B	2242	S2, D2, S3, D3, D5	B+M
	N/A	N/A	N/A	B	2260	S2, D2, S3, D3, D5	B+M
	N/A	N/A	N/A	B	2280	S2, D2, S3, D3, D5	B+M
	N/A	N/A	N/A	B	22110	S2, D2, S3, D3, D5	B+M
Socket 3 SSD Drive	N/A	N/A	N/A	M	2242	S2, D2, S3, D3, D5	M, B+M
	N/A	N/A	N/A	M	2260	S2, D2, S3, D3, D5	M, B+M
	N/A	N/A	N/A	M	2280	S2, D2, S3, D3, D5	M, B+M
	N/A	N/A	N/A	M	22110	S2, D2, S3, D3, D5	M, B+M

2.3 Socket 3 PCIe-based SSD Module Pinout

74	3.3V	GND	75
72	3.3V	Reserved	73
70	3.3V	GND	71
68	N/C	N/C	69
	Key M	N/C	67
	Key M	Key M	
	Key M	Key M	
	Key M	Key M	
58	Reserved	Key M	
56	Reserved	GND	57
54	N/C	REFCLKp	55
52	3.3V	REFCLKn	53
50	3.3V	GND	51
48	N/C	PERp0	49
46	N/C	PERn0	47
44	N/C	GND	45
42	N/C	PETp0	43
40	N/C	PETn0	41
38	N/C	GND	39
36	N/C	PERp1	37
34	N/C	PERn1	35
32	N/C	GND	33
30	Reserved	PETp1	31
28	N/C	PETn1	29
26	N/C	GND	27
24	N/C	PERp2	25
22	Reserved	PERn2	23
20	N/C	GND	21
18	3.3V	PETp2	19
16	3.3V	PETn2	17
14	3.3V	GND	15
12	3.3V	PERp3	13
10	LED#	PERn3	11
8	Reserved	GND	9
6	N/C	PETp3	7
4	3.3V	PETn3	5
2	3.3V	GND	3
		GND	1

3 PCI EXPRESS

3.1 Interface

The PCI Express interface supports the x1 PCI Express interface (one Lane). A Lane consists of an input and an output high-speed differential pair. Also supported is a PCI Express reference clock. Refer to the PCI Express Base Specification for more details on the functional requirements for the PCI Express interface signals.

Socket 1 pin out has provisions for an additional PCI Express lane indicated by the suffix 1 to the signal names. These additional PETx1 and PERx1 signal sets can serve as the second Lane to the original PCI Express interface, or alternatively, they can be complimented with a second set of REFCLKx1 and a set of Auxiliary Signals on the adjacent reserved pins to form a complete second PCI Express x1 interface.

3.2 Auxiliary Signals

The auxiliary signals are provided on the system connector to assist with certain system level functionality or implementation. These signals are not required by the PCI Express architecture, but may be required by specific implementations such as PCI Express M.2 Card. The high-speed signal voltage levels are compatible with advanced silicon processes. The optional low speed signals are defined to use the +3.3V supply, as it is the lowest common voltage available. Most ASIC processes have high voltage (thick gate oxide) I/O transistors compatible with +3.3V. The use of the +3.3V supply allows PCI Express signaling to be used with existing control bus structures, avoiding a buffered set of signals and bridges between the buses.

The PCI Express M.2 Card add-in card and system connectors support the auxiliary signals that are described in the following sections.

3.3 Reference Clock

The REFCLK+/REFCLK- signals are used to assist the synchronization of the card's PCI Express interface timing circuits. Availability of the reference clock at the card interface may be gated by the CLKREQ# signal as described in section 3.1.5.1, CLKREQ# Signal. When the reference clock is not available, it will be in the parked state. A parked state is when the clock is not being driven by a clock driver and both REFCLK+ and REFCLK- are pulled to ground by the ground termination resistors. Refer to the PCI Express Card Electromechanical Specification for more details on the functional and tolerance requirements for the reference clock signals.

3.3.1 CLKREQ# Signal

The CLKREQ# signal is an open drain, active low signal that is driven low by the PCI Express M.2 add-I Card function to request that the PCI Express reference clock be available (active clock state) in order to allow the PCI Express interface to send/receive data. Operation of the CLKREQ# signal is determined by the state of the Enable Clock Power Management bit in the Link Control Register (offset 010h). When disabled, the CLKREQ# signal shall be asserted at all times whenever power is applied to the card, with the exception that it may be de-asserted during L1 PM Sub states. When enabled, the CLKREQ# signal may be de-asserted during the L1 Link state.

The CLKREQ# signal is also used by the L1 PM Sub states mechanism. In this case, CLKREQ# can be asserted by either the system or add-in card to initiate an L1 exit. See the PCI Express Base Specification for details on the functional requirements for the CLKREQ# signal when implementing L1 PM Sub states.

Whenever dynamic clock management is enabled and when a card stops driving CLKREQ# low, it indicates that the device is ready for the reference clock to transition from the active clock state to a parked (not available) clock state. Reference clocks are not guaranteed to be parked by the host system when CLKREQ# gets de-asserted and module designs shall be tolerant of an active reference clock even when CLKREQ# is de-asserted by the module.

The card must drive the CLKREQ# signal low during power up, whenever it is reset, and whenever it requires the reference clock to be in the active clock state. Whenever PERST# is asserted, including when the device is not in D0, CLKREQ# shall be asserted.

It is important to note that the PCI Express device must delay de-assertion of its CLKREQ# signal until it is ready for its reference clock to be parked. The device must be able to assert its clock request signal, whether or not the reference clock is active or parked, when it needs to put its Link back into the L0 Link state. Finally, the device must be able to sense an electrical idle break on its up-stream-directed receive port and assert its clock request, whether or not the reference clock is active or parked.

The assertion and de-assertion of CLKREQ# are asynchronous with respect to the reference clock. Add-in cards that do not implement a PCI Express interface shall leave this output unconnected on the card. CLKREQ# has additional electrical requirements over and above standard open drain signals that allow it to be shared between devices that are powered off and other devices that may be powered on. The additional requirements include careful circuit design to ensure that a voltage applied to the CLKREQ# signal network never causes damage to a component even if that particular component’s power is not applied.

Additionally, the device must ensure that it does not pull CLKREQ# low unless CLKREQ# is being intentionally asserted in all cases; including when the related function is in D3cold. This means that any component implementing CLKREQ# must be designed such that:

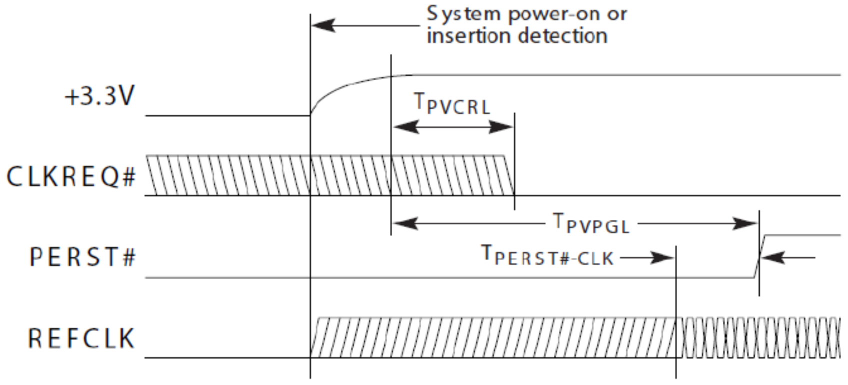
-Unpowered CLKREQ# output circuits are not damaged if a voltage is applied to them from other powered "wire-Red" sources of CLKREQ#.

-When power is removed from its CLKREQ# generation logic, the unpowered output does not present a low impedance path to ground or any other voltage.

These additional requirements ensure that the CLKREQ# signal network continues to function properly when a mixture of powered and unpowered components have their CLKREQ# outputs wire-ORed together. It is important to note that most commonly available open drain and tri-state buffer circuit designs used "as is" do not satisfy the additional circuit design requirements for CLKREQ#.

3.3.2 Power-up Requirements

CLKREQ# is asserted in response to PERST# assertion. On power up, CLKREQ# must be asserted by a PCI Express device within a delay (TPVCRL) from the power rails achieving specified operating limits and PERST# assertion (see below Figure). This delay is to allow adequate time for the power to stabilize on the card and certain system functions to start prior to the card starting up. CLKREQ# may not be de-asserted while PERST# is asserted.



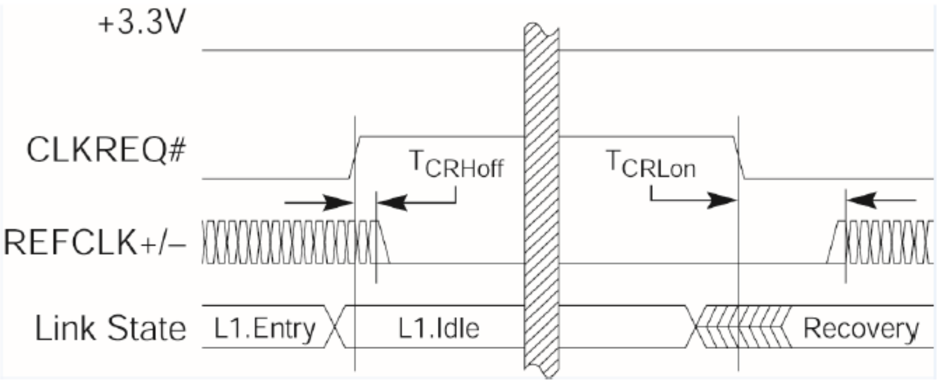
Note: T_{PVCRL} is measured from the later rising edge of +3.3V.

3.3.3 Dynamic Clock Control

After a PCI Express device has powered up and whenever its upstream link enters the L1 link state, it shall allow its reference clock to be turned off (put into the parked clock state). To accomplish this, the device de-asserts CLKREQ# (high) and must allow that the reference clock will transition to the parked clock state within a delay (TCRHoff). Figure 79 shows the CLKREQ# clock control timing diagram.

To exit L1, the device must assert CLKREQ# (low) to re-enable the reference clock. After the device asserts CLKREQ# (low) it must allow that the reference clock will continue to be in the parked clock state for a delay (TCRLon) before transitioning to the active clock state. The time that it takes for the device to assert CLKREQ# and for the system to return the reference clock to the active clock state are serialized with respect to the remainder of L1 recovery. This time must be taken into account when the device is reporting its L1 exit latency.

When the PCI Express device supports, and is enabled for, Latency Tolerance Reporting (LTR), the device must allow that the reference clock transition to the active clock state may be additionally delayed by the system up to a maximum value consistent with requirements for the LTR mechanism. During this delay, the reference clock must remain parked. When exiting the parked state following the delay, the clock must be stable and valid within 400 ns.



3.3.4 Clock Request Support Reporting and Enabling

Support for the CLKREQ# dynamic clock protocol should be reported using bit 18 in the PCI Express link capabilities register (offset 0C4h). To enable dynamic clock management, bit 8 of the Link Control register (offset 010h) is provided. By default, the card shall enable CLKREQ# dynamic clock protocol upon initial power up and in response to any warm reset by the host system. System software may subsequently disable this feature as needed. Refer to the PCI Express Base Specification, Revision 1.1 (or later) for more information regarding these bits.

3.3.5 PERST# Signal

- The PERST# signal is de-asserted to indicate when the system power sources are within their specified voltage tolerance and are stable.
- PERST# should be used to initialize the card functions once power sources stabilize.
- PERST# is asserted when power is switched off and also can be used by the system to force a hardware reset on the card.
- System may use PERST# to cause a warm reset of the add-in card.

Refer to the PCI Express Card Electromechanical Specification for more details on the functional requirements for the PERST# signal.

4 ADMIN COMMAND SETS

4.1 Admin Command

The CL4-4DXXX PCIe Gen4 x 4 Lane SSD supports all the mandatory Admin commands defined in the NVMe 1.4 specification which consists of

- Delete I/O Submission Queue
- Create I/O Submission Queue
- Get Log Page
- Delete I/O Completion Queue
- Create I/O Completion Queue
- Identify
- Abort
- Set Features
- Get Features
- Asynchronous Event Request

The CL4-4DXXX PCIe Gen4 x 4 Lane SSD supports all the following optional commands

- Firmware Commit
- Firmware Image Download
- Security Send
- Security Receive
- Device Self-test
- Format NVM
- Sanitize

4.2 Namespace Feature Set

CL4 without support this feature set.

4.3 Security Feature Set

The Security Receive command transfers the status and data result of one or more Security Send commands that were previously submitted to the controller.

The association between a Security Receive command and previous Security Send commands is dependent on the Security Protocol. The format of the data to be transferred is dependent on the Security Protocol. Refer to SPC-4 for Security Protocol details.

Each Security Receive command returns the appropriate data corresponding to a Security Send command as defined by the rules of the Security Protocol. The Security Receive command data may not be retained if there is a loss of communication between the controller and host, or if a controller reset occurs.

The Security Send command is used to transfer security protocol data to the controller. The data structure transferred to the controller as part of this command contains security protocol specific commands to be performed by the controller. The data structure transferred may also contain data or parameters associated with the security protocol commands. Status and data that is to be returned to the host for the security protocol commands submitted by a Security Send command are retrieved with the Security Receive command.

5 NVME COMMAND SETS

5.1 NVMe Command

The CL4-4DXXX PCIe Gen4 x 4 Lane SSD supports all the mandatory NVMe commands defined in the NVMe 1.4 specification, which consists of

- Flush
- Write
- Read

The CL4-4DXXX PCIe Gen4 x 4 Lane SSD supports all the following optional commands

- Write Uncorrectable
- Dataset Management
- Write Zeroes
- Verify

5.2 Power Management Feature Set

The power management capability allows the host to manage NVM subsystem power statically or dynamically. Static power management consists of the host determining the maximum power that may be allocated to an NVM subsystem and setting the NVM Express power state to one that consumes this amount of power or less. Dynamic power management consists of the host modifying the NVM Express power state to best satisfy changing power and performance objectives. This power management mechanism is meant to complement and not replace autonomous power management performed by a controller.

Associated with each power state is a Power State Descriptor in the Identify Controller data structure. The descriptors for all implemented power states may be viewed as forming a table as shown for a controller with three implemented power states. The Maximum Power (MP) field indicates the instantaneous maximum power that may be consumed in that state. The controller may employ autonomous power management techniques to reduce power consumption below this level, but under no circumstances is power allowed to exceed this level.

5.3 Host Memory Buffer

The Host Memory Buffer feature allows the controller to utilize an assigned portion of host memory exclusively. The use of the host memory resources is vendor specific. Host software may not be able to provide any or a limited amount of the host memory resources requested by the controller. The controller shall function properly without host memory resources.

During initialization, host software may provide a descriptor list that describes a set of host memory address ranges for exclusive use by the controller. The host memory resources assigned are for the exclusive use of the controller (host software should not modify the ranges) until host software requests that the controller release the ranges and the controller completes the Set Features command. The controller is responsible for initializing the host memory resources. Host software should request that the controller release the assigned ranges prior to a shutdown event, a Runtime D3 event, or any other event that requires host software to reclaim the assigned ranges. After the controller acknowledges that it is no longer using the ranges, host software may reclaim the host memory resources. In the case of Runtime D3, host software should provide the host memory resources to the controller again and inform the controller that the ranges were in use prior to the RTD3 event and have not been modified. The host memory resources are not persistent in the controller across a reset event. Host software should provide the previously allocated host memory resources to the controller after the reset completes. If host software is providing previously allocated host memory resources (with the same contents) to the controller, the Memory Return bit is set to '1' in the Set Features command.

The controller shall ensure that there is no data loss or data corruption in the event of a surprise removal while the Host Memory Buffer feature is being utilized.

6 REFERENCES

This document references standards defined by a variety of organizations as listed below.

Table 55 Standards References

Title	Location
VCCI	http://www.vcci.or.jp/vcci_e/general/join/index.html
ROHS	Search for material description datasheet at http://intel.pcnalert.com
SFF-8144, 1.8” drive form factor	http://www.sffcommittee.org
PCI Express Specification	http://www.pcisig.com
SFF-8223, 2.5” Drive w/Serial Attachment Connector	http://www.sffcommittee.org
SFF-8201, 2.5” drive form factor	http://www.sffcommittee.org
NVM Express Specification	http://www.nvmexpress.org
International Electro Technical Commission EB61000 4-2 Personnel Electrostatic Discharge Immunity 4-3 Electromagnetic compatibility (EMC) 4-4 Electromagnetic compatibility (EMC) 4-5 Electromagnetic compatibility (EMC) 4-6Electromagnetic compatibility (EMC) 4-11 (Voltage variations)	http://www.iec.ch
ENV 50204 (Radiated electromagnetic field from digital radio telephones)	http://www.iec.ch

7 TERMS AND ACRONYMS

This document incorporates many industry- and device-specific words use the following list to define a variety of terms and acronyms.

Table 66 Glossary of Terms and Acronyms

Term	Definition
BER	Bit Error Rate, or percentage of bits that have errors relative to the total number of bits received
BIOS	Basic Input/Output System
Chipset	A term used to define a collection of integrated components required to make a PC function
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
EXT	Extended
FP	First Party
GB	Giga-byte defined as $1X10^9$ bytes
HCI	Host Controller Interface
HCT	Hardware Compatibility Test
HDD	Hard Disk Drive
IOPS	Input output operations per second
LBA	Logical Block Address
MB	Mega-bytes defined as $1x10^6$ bytes
mSATA	Mini-SATA
MTBF	Mean time between failure
NCQ	Native Command Queuing The ability of the SATA hard drive to re-order commands in order to maximize the efficiency of gathering data from the platters
NOP	No operation
NTFS	NT file system
OEM	Original Equipment Manufacturer
OS	Operation System
Port	The point at which a SATA drive physically connected to the SATA controller
RAID	Redundant Array of Independent Disks
RMS	Root Mean Squared
RPM	Revolutions per Minute
RTM	Release to Manufacture
SATA	Serial ATA
SFF	Small Form Factor
SMART	Self-Monitoring, Analysis and reporting Technology An open standard for developing hard drive and software systems that automatically monitors a hard drive's health and reports potential problems

SSD	Solid State Drive
TBD	To Be Determined
WHQL	Microsoft* Windows Hardware Quality Labs
Write Cache	A memory device within a hard drive, which is allocated for the temporary storage of data before that data is copied to its permanent storage location
VCCI	Voluntary Control Council for Interface
A	Amperage or Amp
DC	Direct Current
GND	Ground
GNSS	Global Navigation Satellite System (GPS+GLONASS)
HDR	Hybrid Digital Radio
HSIC	High Speed Inter-Chip
I/F	Interface
I/O	Input/Output
IR	Current x Resistance = Voltage
I2C	Inter-Integrated Circuit
I2S	Integrated Interchip Sound
LED	Light Emitting Diode
LGA	Laned Grid Array
mΩ	milli Ohm
mA	milli Amp
mV	milli Volt
NFC	Near Field Communications
M.2	Formally called Next Generation Form Factor (NGFF)
NB	Notebook
NIC	Network Interface Card
NC	Not Connected
SATA	Serial Advanced Technology Attachment or Serial ATA
PCIe	Peripheral Component Interconnect Express
PCM	Pulse Code Modulation
SDIO	Secure Digital Input Output
SIM	Subscriber Identity Module
SSD	Sold-State Storage Device
RF	Radio Frequency
RM	Root Mean Square
RoHS	Restriction of Hazardous Substances Directive
RTC	Real Time Clock
RFU	Reserved for Future Use
UIM	User Identity Module
UART	Universal Asynchronous Receive Transmit
W	Wattage or Watts
WiGig	Wireless Giga communication
WLANE	Wireless Local Area Network
WPAN	Wireless Personal Area Network
WWAN	Wireless Wide Area Network
V	Voltage