

# Advantech

## AQD-D4U16GN32-SE Datasheet

Rev. 0.0

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## Description

AQD-D4U16GN32-SE is a DDR4 3200Mbps U-DIMM high-speed, memory module that use 16pcs of 1024Mx 8 bits DDR4 SDRAM in FBGA package and a 4K bits serial EEPROM on a 288-pin printed circuit board.

AQD-D4U16GN32-SE is a Dual In-Line Memory Module and is intended for mounting into 288-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

## Features

- RoHS compliant products.
- JEDEC standard 1.2V(1.14V~1.26V) Power supply  
VDDQ= 1.2V(1.14V~1.26V)
- VPP = 2.5V +0.25V / -0.125V
- Data transfer rates: PC4-3200  
Programmable CAS Latency:11,12,13,14,15,16,17~22
- 8 bit pre-fetch
- Burst Length (BL) switch on-the-fly BL8 or BC4
- Bi-directional Differential Data-Strobe
- On Die Termination, Nominal, Park, and Dynamic ODT
- Serial presence detect with EEPROM  
Asynchronous reset  
PCB edge connector treated with 30u" Gold-Plating
- Anti - sulfur resistor used

## Pin Identification

| Symbol                        | Function               |
|-------------------------------|------------------------|
| A0~A17 <sup>1</sup> , BA0~BA1 | Address/Bank input     |
| DQ0~DQ63                      | Bi-direction data bus. |

|                    |  |
|--------------------|--|
| DQS0_t~DQS17_t     | Data Buffer data strobes                 |
| DQS0_c~DQS17_c     | Data Buffer data strobes                 |
| CK0_t, CK1_t       | SDRAM clocks                             |
| CK0_c, CK1_c       | SDRAM clocks                             |
| ODT0 &ODT1         | On-die termination control line          |
| CS0_n~CS3_n        | DIMM Rank Select Lines input.            |
| RAS_n <sup>2</sup> | Row address strobe                       |
| CAS_n <sup>3</sup> | Column address strobe                    |
| WE_n <sup>4</sup>  | Write Enable                             |
| DM0~DM7            | Data masks/high data strobes             |
| VDD                | Core power supply                        |
| VDDQ               | I/O driver power supply                  |
| V <sub>REFCA</sub> | Command/address reference supply         |
| V <sub>DDSPD</sub> | SPD EEPROM power supply                  |
| SA0~SA2            | I2C serial bus address select for EEPROM |
| SCL                | I2C serial bus clock for EEPROM          |
| SDA                | I2C serial bus data for EEPROM           |
| VSS                | Ground                                   |
| RESET_n            | Set DRAMs Known State                    |
| VTT                | DRAM I/O termination supply              |
| VPP                | SDRAM Supply                             |
| ALERT_n            | SDRAM ALERT_n                            |
| EVENT_n            | SPD signals a thermal event has occurred |
| RFU                | Reserved for future use                  |

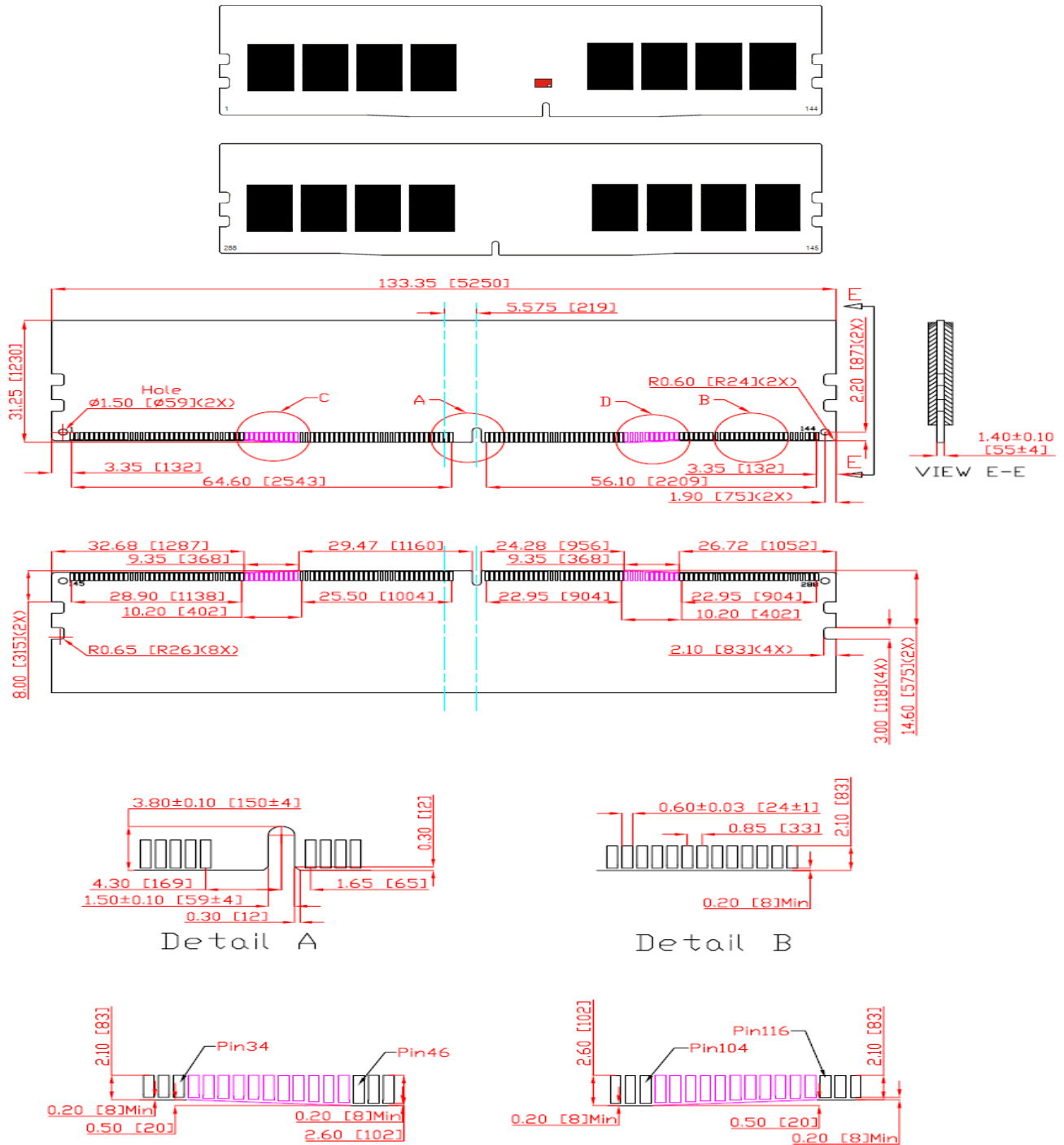
1. Address A17 is not valid for x8 and x16 based SDRAMs. For UDIMMs this connection pin is NC.

2. RAS\_n is a multiplexed function with A16.

3. CAS\_n is a multiplexed function with A15.

4. WE\_n is a multiplexed function with A14.

Dimensions (Unit: millimeter)



Detail A  
Detail B  
Detail C  
Detail D  
Note:1. Tolerances on all dimensions +/-0.15mm unless otherwise specified.



Enabling an Intelligent Planet

288Pin DDR4 3200 1.2V U-DIMM

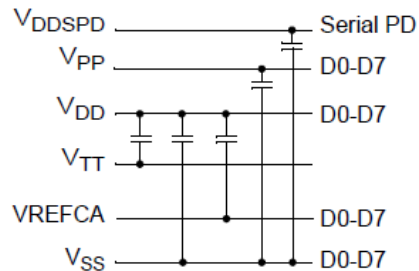
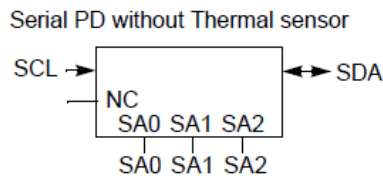
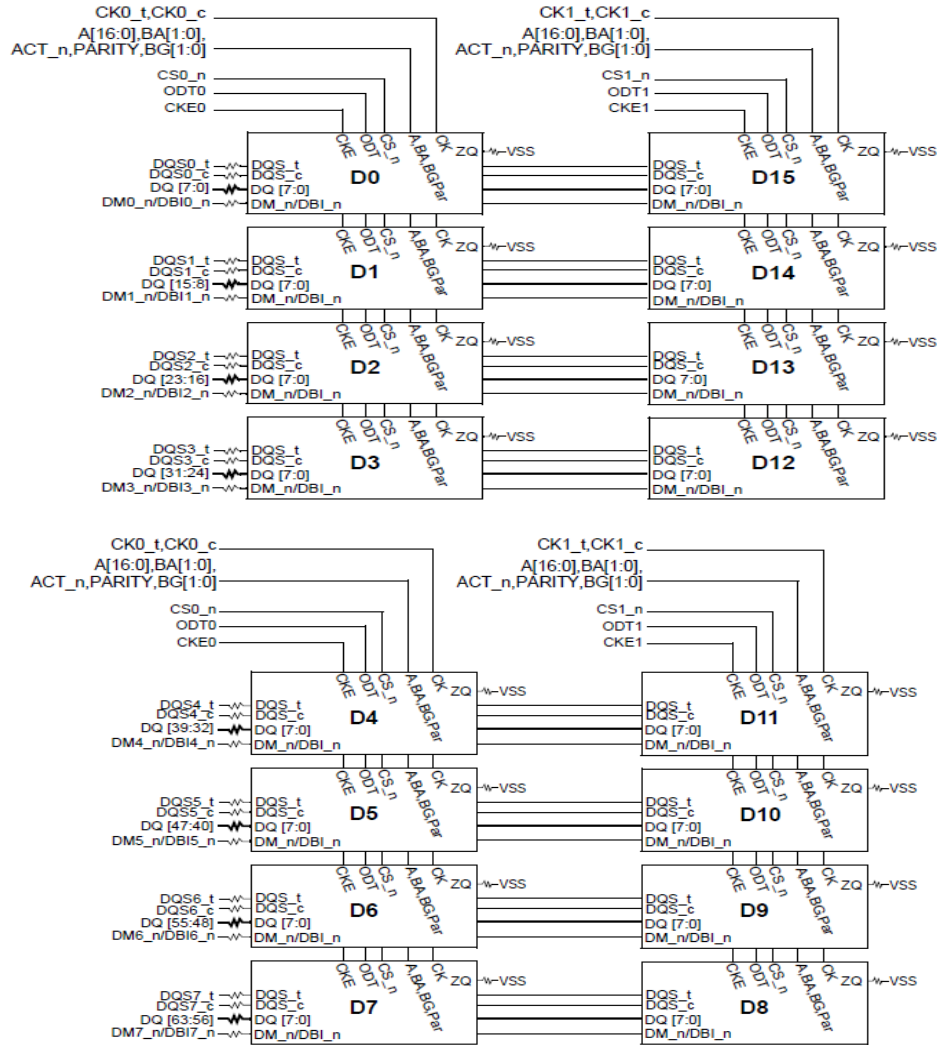
16GB Based on 1024Mx8

AQD-D4U16GN32-SE

Pin Assignments

| Pin | Front    | Pin | Front    | Pin | Front     | Pin | Back     | Pin | Back  | Pin | Back     | Pin | Back  | Pin | Back   |
|-----|----------|-----|----------|-----|-----------|-----|----------|-----|-------|-----|----------|-----|-------|-----|--------|
| 1   | 12V      | 41  | NC       | 81  | BA0       | 121 | DM6,DBI6 | 161 | DQ9   | 201 | CB3      | 241 | VSS   | 281 | VSS    |
| 2   | VSS      | 42  | VSS      | 82  | RAS_n/A16 | 122 | NC       | 162 | VSS   | 202 | VSS      | 242 | DQ33  | 282 | DQ59   |
| 3   | DQ4      | 43  | DQ30     | 83  | VDD       | 123 | VSS      | 163 | DQS1C | 203 | CKE1     | 243 | VSS   | 283 | VSS    |
| 4   | VSS      | 44  | VSS      | 84  | CS0_n     | 124 | DQ54     | 164 | DQS1T | 204 | VDD      | 244 | DQS4C | 284 | VDDSPD |
| 5   | DQ0      | 45  | DQ26     | 85  | VDD       | 125 | VSS      | 165 | VSS   | 205 | RFU      | 245 | DQS4T | 285 | SDA    |
| 6   | VSS      | 46  | VSS      | 86  | CAS_n/A15 | 126 | DQ50     | 166 | DQ15  | 206 | VDD      | 246 | VSS   | 286 | VPP    |
| 7   | DM0,DBI0 | 47  | CB4      | 87  | ODT0      | 127 | VSS      | 167 | VSS   | 207 | BG1      | 247 | DQ39  | 287 | VPP    |
| 8   | NC       | 48  | VSS      | 88  | VDD       | 128 | DQ60     | 168 | DQ11  | 208 | ALERT_n  | 248 | VSS   | 288 | VPP    |
| 9   | VSS      | 49  | CB0      | 89  | CS1_n     | 129 | VSS      | 169 | VSS   | 209 | VDD      | 249 | DQ35  |     |        |
| 10  | QD6      | 50  | VSS      | 90  | VDD       | 130 | DQ56     | 170 | DQ21  | 210 | A11      | 250 | VSS   |     |        |
| 11  | VSS      | 51  | DM8,DBI8 | 91  | ODT1      | 131 | VSS      | 171 | VSS   | 211 | A7       | 251 | DQ45  |     |        |
| 12  | DQ2      | 52  | NC       | 92  | VDD       | 132 | DM7,DBI7 | 172 | DQ17  | 212 | VDD      | 252 | VSS   |     |        |
| 13  | VSS      | 53  | VSS      | 93  | NC        | 133 | NC       | 173 | VSS   | 213 | A5       | 253 | DQ41  |     |        |
| 14  | DQ12     | 54  | CB6      | 94  | VSS       | 134 | VSS      | 174 | DQS2C | 214 | A4       | 254 | VSS   |     |        |
| 15  | VSS      | 55  | VSS      | 95  | DQ36      | 135 | DQ62     | 175 | DQS2T | 215 | VDD      | 255 | DQS5C |     |        |
| 16  | DQ8      | 56  | CB2      | 96  | VSS       | 136 | VSS      | 176 | VSS   | 216 | A2       | 256 | DQS5T |     |        |
| 17  | VSS      | 57  | VSS      | 97  | DQ32      | 137 | DQ58     | 177 | DQ23  | 217 | VDD      | 257 | VSS   |     |        |
| 18  | DM1,DBI1 | 58  | RESET_n  | 98  | VSS       | 138 | VSS      | 178 | VSS   | 218 | CK1T     | 258 | DQ47  |     |        |
| 19  | NC       | 59  | VDD      | 99  | DM4,DBI4  | 139 | SA0      | 179 | DQ19  | 219 | CK1C     | 259 | VSS   |     |        |
| 20  | VSS      | 60  | CKE0     | 100 | NC        | 140 | SA1      | 180 | VSS   | 220 | VDD      | 260 | DQ43  |     |        |
| 21  | DQ14     | 61  | VDD      | 101 | VSS       | 141 | SCL      | 181 | DQ29  | 221 | VTT      | 261 | VSS   |     |        |
| 22  | VSS      | 62  | ACT_n    | 102 | DQ38      | 142 | VPP      | 182 | VSS   | 222 | PARITY   | 262 | DQ53  |     |        |
| 23  | DQ10     | 63  | BG0      | 103 | VSS       | 143 | VPP      | 183 | DQ25  | 223 | VDD      | 263 | VSS   |     |        |
| 24  | VSS      | 64  | VDD      | 104 | DQ34      | 144 | RFU      | 184 | VSS   | 224 | BA1      | 264 | DQ49  |     |        |
| 25  | DQ20     | 65  | A12/BC_n | 105 | VSS       | 145 | 12V      | 185 | DQS3C | 225 | A10_AP   | 265 | VSS   |     |        |
| 26  | VSS      | 66  | A9       | 106 | DQ44      | 146 | VREFCA   | 186 | DQS3T | 226 | VDD      | 266 | DQS6C |     |        |
| 27  | DQ16     | 67  | VDD      | 107 | VSS       | 147 | VSS      | 187 | VSS   | 227 | RFU      | 267 | DQS6T |     |        |
| 28  | VSS      | 68  | A8       | 108 | DQ40      | 148 | DQ8      | 188 | DQ31  | 228 | WE_n/A14 | 268 | VSS   |     |        |
| 29  | DM2,DBI2 | 69  | A6       | 109 | VSS       | 149 | VSS      | 189 | VSS   | 229 | VDD      | 269 | DQ55  |     |        |
| 30  | NC       | 70  | VDD      | 110 | DM5,DBI5  | 150 | DQ1      | 190 | DQ27  | 230 | NC       | 270 | VSS   |     |        |
| 31  | VSS      | 71  | A3       | 111 | NC        | 151 | VSS      | 191 | VSS   | 231 | VDD      | 271 | DQ51  |     |        |
| 32  | DQ22     | 72  | A1       | 112 | VSS       | 152 | DQS0C    | 192 | CB5   | 232 | A13      | 272 | VSS   |     |        |
| 33  | VSS      | 73  | VDD      | 113 | DQ46      | 153 | DQS0T    | 193 | VSS   | 233 | VDD      | 273 | DQ61  |     |        |
| 34  | DQ18     | 74  | CK0T     | 114 | VSS       | 154 | VSS      | 194 | CB1   | 234 | NC       | 274 | VSS   |     |        |
| 35  | VSS      | 75  | CK0C     | 115 | DQ42      | 155 | DQ7      | 195 | VSS   | 235 | NC       | 275 | DQ57  |     |        |
| 36  | DQ28     | 76  | VDD      | 116 | VSS       | 156 | VSS      | 196 | DQS8C | 236 | VDD      | 276 | VSS   |     |        |
| 37  | VSS      | 77  | VTT      | 117 | DQ52      | 157 | DQ3      | 197 | DQS8T | 237 | NC       | 277 | DQS7C |     |        |
| 38  | DQ24     | 78  | EVENT_n  | 118 | VSS       | 158 | VSS      | 198 | VSS   | 238 | SA2      | 278 | DQS7T |     |        |
| 39  | VSS      | 79  | A0       | 119 | DQ48      | 159 | DQ13     | 199 | CB7   | 239 | VSS      | 279 | VSS   |     |        |
| 40  | DM3,DBI3 | 80  | VDD      | 120 | VSS       | 160 | VSS      | 200 | VSS   | 240 | DQ37     | 280 | DQ63  |     |        |

## 16GB, 1Gx8 Module (2 Rank x8)



- This technical information is based on industry standard data and tests believed to be reliable. However, Advantech makes no warranties, either expressed or implied, as to its accuracy and assume no liability in connection with the use of this product. Advantech reserves the right to make changes in specifications at any time without prior notice.

### Operating Temperature Condition

| Parameter             | Symbol | Rating  | Unit | Note |
|-----------------------|--------|---------|------|------|
| Operating Temperature | TOPER  | 0 to 85 | °C   | 1,2  |

Note: Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

### Absolute Maximum DC Ratings

| Parameter                           | Symbol    | Value      | Unit | Note |
|-------------------------------------|-----------|------------|------|------|
| Voltage on VDD relative to Vss      | VDD       | -0.3 ~ 1.5 | V    | 1    |
| Voltage on VDDQ pin relative to Vss | VDDQ      | -0.3 ~ 1.5 | V    | 1    |
| Voltage on any pin relative to Vss  | VIN, VOUT | -0.3 ~ 1.5 | V    | 1    |
| Storage temperature                 | TSTG      | -55~+100   | °C   | 1,2  |

Note: 1. Stress greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.  
 2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

### AC & DC Operating Conditions

#### Recommended DC operating conditions

| Parameter                       | Symbol                  | Voltage | Rating           |          |                  | Unit | Notes |
|---------------------------------|-------------------------|---------|------------------|----------|------------------|------|-------|
|                                 |                         |         | Min              | Typ.     | Max              |      |       |
| Supply voltage                  | VDD                     | 1.2V    | 1.14             | 1.2      | 1.26             | V    | 1,2,3 |
| Supply voltage for Output       | VDDQ                    | 1.2V    | 1.14             | 1.2      | 1.26             | V    | 1,2,3 |
| I/O Reference Voltage (DQ)      | VREF <sub>DQ</sub> (DC) | 1.2V    | 0.49*VDD         | 0.50*VDD | 0.51*VDD         | V    | 4     |
| I/O Reference Voltage (CMD/ADD) | VREF <sub>CA</sub> (DC) | 1.2V    | 0.49*VDD         | 0.50*VDD | 0.51*VDD         | V    | 4     |
| AC Input Logic High             | V <sub>IH</sub> (AC)    | 1.2V    | VREF+90          | -        | VDD <sup>2</sup> | mV   |       |
| AC Input Logic Low              | V <sub>IL</sub> (AC)    | 1.2V    | VSS <sup>2</sup> | -        | VREF-90          | mV   |       |
| DC Input Logic High             | V <sub>IH</sub> (DC)    | 1.2V    | VREF+65          | -        | VDD              | mV   |       |
| DC Input Logic Low              | V <sub>IL</sub> (DC)    | 1.2V    | VSS              | -        | VREF-65          | mV   |       |

Note: (1) Under all conditions VDDQ must be less than or equal to VDD.  
 (2) VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.  
 (3) The DC bandwidth is limited to 20MHz.  
 (4) The AC peak noise on VREF may not allow VREF to deviate from VREF(DC) by more than ±1% VDD (for reference: approx. ±12mV)

**IDD Specification parameters Definition - 16GB (2 Rank x8)**

| Parameter   | Symbol              | DDR4 3200 CL22 | Unit |
|---|---------------------|----------------|------|
| One bank ACTIVATE-PRECHARGE current                       | IDD0 <sup>1</sup>   | 352            | mA   |
| One bank ACTIVATE-PRECHARGE, wordline boost, IPP current  | IPP0 <sup>1</sup>   | 64             | mA   |
| One Bank Active-Read-Precharge Current                    | IDD1 <sup>1</sup>   | 376            | mA   |
| Precharge Standby Current                                 | IDD2N <sup>2</sup>  | 320            | mA   |
| Precharge standby ODT current                             | IDD2NT <sup>1</sup> | 280            | mA   |
| Precharge Power-Down Current                              | IDD2P <sup>2</sup>  | 208            | mA   |
| Precharge Quiet Standby Current                           | IDD2Q <sup>2</sup>  | 320            | mA   |
| Active standby current                                    | IDD3N <sup>2</sup>  | 480            | mA   |
| Active standby IPP current                                | IPP3N <sup>2</sup>  | 64             | mA   |
| Active Power-Down Current                                 | IDD3P <sup>2</sup>  | 336            | mA   |
| Burst Read Current  | IDD4R <sup>1</sup>  | 1016           | mA   |
| Burst write current                                       | IDD4W <sup>1</sup>  | 952            | mA   |
| Burst refresh current (1x REF)                            | IDD5B <sup>1</sup>  | 1944           | mA   |
| Burst refresh IPP current (1x REF)                        | IPP5B <sup>1</sup>  | 232            | mA   |
| Self refresh current: Normal temperature range (0–85°C)   | IDD6N <sup>2</sup>  | 336            | mA   |
| Self refresh current: Extended temperature range (0–95°C) | IDD6E <sup>2</sup>  | 512            | mA   |
| Bank interleave read current                              | IDD7 <sup>1</sup>   | 1368           | mA   |
| Bank interleave read IPP current                          | IPP7 <sup>1</sup>   | 120            | mA   |
| Maximum power-down current                                | IDD8 <sup>2</sup>   | 176            | mA   |

Note: 1. One module rank in the active IDD/PP, the other rank in IDD2P/PP3N.  
 2. All ranks in this IDD/PP condition.  
 3. IDD current measure method and detail patterns are described on DDR4 component datasheet. Only for reference.

■ Timing Parameters & Specifications

| Parameter   | Symbol                    | DDR4-2400  |  | DDR4-2666 |        | DDR4-2933 |       | DDR4-3200 |        | Unit     | Notes |         |
|---|---------------------------|--|--|-----------|--------|-----------|-------|-----------|--------|----------|-------|---------|
|   |                           | Min  | Max  | Min       | Max    | Min       | Max   | Min       | Max    |          |       |         |
| <b>Clock Timing</b>   |                           |  |  |           |        |           |       |           |        |          |       |         |
| Clock period average(DLL off mode)                          | tCK(DLL_OFF)              | 8  | 20   | 8         | 20     | 8         | 20    | 8         | 20     | ns       |       |         |
| Clock period average  | tCK(AVG)<br>(DLL_ON)      | 0.833  | <0.938   | 0.75      | <0.833 | 0.682     | <0.75 | 0.625     | <0.682 | ns       | 14    |         |
| High pulse width average                                    | tCH (AVG)                 | 0.48   | 0.52   | 0.48      | 0.52   | 0.48      | 0.52  | 0.48      | 0.52   | tCK(AVG) |       |         |
| Low pulse width average                                     | tCL (AVG)                 | 0.48   | 0.52   | 0.48      | 0.52   | 0.48      | 0.52  | 0.48      | 0.52   | tCK(AVG) |       |         |
| Clock period jitter   | Total                     | tJITper_tot  | -42  | 42        | -38    | 38        | -34   | 34        | -32    | 32       | ps    | 18 , 19 |
|   | Deterministic             | tJITper_dj   | -21  | 21        | -19    | 19        | -17   | 17        | -16    | 16       | ps    | 18      |
|   | DLL locking               | tJITper,lck  | -33  | 33        | -30    | 30        | -27   | 27        | -25    | 25       | ps    |         |
| Clock absolute period                                       | tCK (ABS)                 | MIN = tCK (AVG) MIN + tJITper_tot MIN; MAX = tCK (AVG) MAX + tJITper_tot MAX |  |           |        |           |       |           |        | ps       |       |         |
| Clock absolute high pulse width(includes duty cycle jitter) | tCH (ABS)                 | 0.45   | -  | 0.45      | -      | 0.45      | -     | 0.45      | -      | tCK(AVG) |       |         |
| Clock absolute low pulse width(includes duty cycle jitter)  | tCL (ABS)                 | 0.45   | -  | 0.45      | -      | 0.45      | -     | 0.45      | -      | tCK(AVG) |       |         |
| Cycle-to-cycle jitter                                       | Total                     | tJITcc_tot   | -  | 83        | -      | 75        | -     | 68        | -      | 62       | ps    |         |
|   | DLL locking               | tJITcc,lck   | -  | 67        | -      | 60        | -     | 55        | -      | 50       | ps    |         |
| Cumulative error across                                     | 2 cycles                  | tERR2per   | -61  | 61        | -55    | 55        | -50   | 50        | -46    | 46       | ps    |         |
|   | 3 cycles                  | tERR3per   | -73  | 73        | -66    | 66        | -60   | 60        | -55    | 55       | ps    |         |
|   | 4 cycles                  | tERR4per   | -81  | 81        | -73    | 73        | -66   | 66        | -61    | 61       | ps    |         |
|   | 5 cycles                  | tERR5per   | -87  | 87        | -78    | 78        | -71   | 71        | -65    | 65       | ps    |         |
|   | 6 cycles                  | tERR6per   | -92  | 92        | -83    | 83        | -75   | 75        | -69    | 69       | ps    |         |
|   | 7 cycles                  | tERR7per   | -97  | 97        | -87    | 87        | -79   | 79        | -73    | 73       | ps    |         |
|   | 8 cycles                  | tERR8per   | -101   | 101       | -91    | 91        | -83   | 83        | -76    | 76       | ps    |         |
|   | 9 cycles                  | tERR9per   | -104   | 104       | -94    | 94        | -85   | 85        | -78    | 78       | ps    |         |
|   | 10 cycles                 | tERR10per  | -107   | 107       | -96    | 96        | -88   | 88        | -80    | 80       | ps    |         |
|   | 11 cycles                 | tERR11per  | -110   | 110       | -99    | 99        | -90   | 90        | -83    | 83       | ps    |         |
|   | 12 cycles                 | tERR12per  | -112   | 112       | -101   | 101       | -92   | 92        | -84    | 84       | ps    |         |
|   | n=13,14...49,<br>50cycles | tERRnper   | tERRnper MIN = (1 + 0.68ln[n]) × tJITper_tot MIN<br>tERRnper MAX = (1 + 0.68ln[n]) × tJITper_tot MAX |           |        |           |       |           |        |          | ps    |         |



| Parameter  |                                | Symbol               | DDR4-2400   |      | DDR4-2666 |      | DDR4-2933 |      | DDR4-3200 |      | Unit | Notes |
|--|--------------------------------|----------------------|---|------|-----------|------|-----------|------|-----------|------|------|-------|
|  |                                |                      | Min   | Max  | Min       | Max  | Min       | Max  | Min       | Max  |      |       |
| <b>DQ Input Timing</b>   |                                |                      |   |      |           |      |           |      |           |      |      |       |
| Data setup time to<br>DQS_t, DQS_c   | Base(calibrated<br>$V_{REF}$ ) | tDS                  | Refer to DQ Input Receiver Specification section<br>(approximately 0.15tCK to 0.28tCK ) |      |           |      |           |      |           |      | -    |       |
|  | Noncalibrated<br>$V_{REF}$     | tPDA_S               | minimum of 0.5UI  |      |           |      |           |      |           |      | UI   | 23    |
| Data hold time from<br>DQS_t, DQS_c  | Base(calibrated<br>$V_{REF}$ ) | tDS                  | Refer to DQ Input Receiver Specification section<br>(approximately 0.15tCK to 0.28tCK ) |      |           |      |           |      |           |      | -    |       |
|  | Noncalibrated<br>$V_{REF}$     | tPDA_S               | minimum of 0.5UI  |      |           |      |           |      |           |      | UI   | 23    |
| DQ and DM minimum data pulse width<br>for each input                                 |                                | tDIPW                | 0.58  | -    | 0.58      | -    | 0.58      | -    | 0.58      | -    | UI   |       |
| <b>DQ Output Timing (DLL enabled)</b>  |                                |                      |   |      |           |      |           |      |           |      |      |       |
| DQS_t, DQS_c to DQ skew, per group,<br>per access                                    |                                | tDQSQ                | -   | 0.17 | -         | 0.18 | -         | 0.19 | -         | 0.22 | UI   |       |
| DQ output hold time from DQS_t,<br>DQS_c   |                                | tQH                  | 0.74  | -    | 0.74      | -    | 0.74      | -    | 0.74      | -    | UI   |       |
| Data Valid Window per device: tQH<br>-tDQSQ each device's output per UI              |                                | tDVWd                | 0.64  | -    | 0.64      | -    | 0.64      | -    | 0.64      | -    | UI   |       |
| Data Valid Window per device, per pin:<br>tQH - tDQSQ each device's output per<br>UI |                                | tDVWp                | 0.72  | -    | 0.72      | -    | 0.72      | -    | 0.72      | -    | UI   |       |
| DQ Low-Z time from CK_t, CK_c  |                                | tLZDQ                | -330  | 175  | -310      | 170  | -280      | 165  | -250      | 160  | ps   |       |
| DQ High-Z time from CK_t, CK_c   |                                | tHZDQ                | -   | 175  | -         | 170  | -         | 165  | -         | 160  | ps   |       |
| <b>DQ Strobe Input Timing</b>  |                                |                      |   |      |           |      |           |      |           |      |      |       |
| DQS_t, DQS_c rising edge to CK_t,<br>CK_c rising edge for 1tCKpreamble               |                                | tDQSS <sub>1ck</sub> | -0.27   | 0.27 | -0.27     | 0.27 | -0.27     | 0.27 | -0.27     | 0.27 | CK   |       |
| DQS_t, DQS_c rising edge to CK_t,<br>CK_c rising edge for 2tCKpreamble               |                                | tDQSS <sub>2ck</sub> | -0.50   | 0.50 | -0.50     | 0.50 | -0.50     | 0.50 | -0.50     | 0.50 | CK   |       |
| DQS_t, DQS_c differential input low<br>pulse width                                   |                                | tDQSL                | 0.46  | 0.54 | 0.46      | 0.54 | 0.46      | 0.54 | 0.46      | 0.54 | CK   |       |

| Parameter  | Symbol               | DDR4-2400 |      | DDR4-2666 |      | DDR4-2933 |      | DDR4-3200 |      | Unit | Notes |
|--|----------------------|-----------|------|-----------|------|-----------|------|-----------|------|------|-------|
|  |                      | Min       | Max  | Min       | Max  | Min       | Max  | Min       | Max  |      |       |
| <b>DQ Strobe Input Timing</b>                                      |                      |           |      |           |      |           |      |           |      |      |       |
| DQS_t, DQS_c differential input high pulse width                   | tDQSH                | 0.46      | 0.54 | 0.46      | 0.54 | 0.46      | 0.54 | 0.46      | 0.54 | CK   |       |
| DQS_t, DQS_c falling edge setup to CK_t, CK_c rising edge          | tDSS                 | 0.18      | -    | 0.18      | -    | 0.18      | -    | 0.18      | -    | CK   |       |
| DQS_t, DQS_c falling edge hold from CK_t, CK_c rising edge         | tDSH                 | 0.18      | -    | 0.18      | -    | 0.18      | -    | 0.18      | -    | CK   |       |
| DQS_t, DQS_c differential WRITE preamble for 1'CKpreamble          | tWPRE <sub>1ck</sub> | 0.9       | -    | 0.9       | -    | 0.9       | -    | 0.9       | -    | CK   |       |
| DQS_t, DQS_c differential WRITE preamble for 2'CKpreamble          | tWPRE <sub>2ck</sub> | 1.8       | -    | 1.8       | -    | 1.8       | -    | 1.8       | -    | CK   |       |
| DQS_t, DQS_c differential WRITE postamble                          | tWPST                | 0.33      | -    | 0.33      | -    | 0.33      | -    | 0.33      | -    | CK   |       |
| <b>DQS Strobe Output Timing (DLL enabled)</b>                      |                      |           |      |           |      |           |      |           |      |      |       |
| DQS_t, DQS_c rising edge output access time from rising CK_t, CK_c | tDQCK                | -175      | 175  | -170      | 170  | -165      | 165  | -160      | 160  | ps   |       |
| DQS_t, DQS_c rising edge output variance window per DRAM           | tDQCKi               | -         | 290  | -         | 270  | -         | 265  | -         | 260  | ps   |       |
| DQS_t, DQS_c differential output high time                         | tQSH                 | 0.4       | -    | 0.4       | -    | 0.4       | -    | 0.4       | -    | CK   |       |
| DQS_t, DQS_c differential output low time                          | tQSL                 | 0.4       | -    | 0.4       | -    | 0.4       | -    | 0.4       | -    | CK   |       |
| DQS_t, DQS_c Low-Z time (RL - 1)                                   | tLZDQS               | -330      | 175  | -310      | 170  | -280      | 165  | -250      | 160  | ps   |       |
| DQS_t, DQS_c High-Z time (RL + BL/2)                               | tHZDQS               | -         | 175  | -         | 170  | -         | 165  | -         | 160  | ps   |       |
| DQS_t, DQS_c differential READ preamble for 1'CKpreamble           | tRPRE <sub>1ck</sub> | 0.9       | -    | 0.9       | -    | 0.9       | -    | 0.9       | -    | CK   |       |
| DQS_t, DQS_c differential READ preamble for 2'CKpreamble           | tRPRE <sub>2ck</sub> | 1.8       | -    | 1.8       | -    | 1.8       | -    | 1.8       | -    | CK   |       |
| DQS_t, DQS_c differential READ postamble                           | tRPST                | 0.33      | -    | 0.33      | -    | 0.33      | -    | 0.33      | -    | CK   |       |

| Parameter  | Symbol             | DDR4-2400                     |           | DDR4-2666                     |           | DDR4-2933                     |           | DDR4-3200                     |           | Unit | Notes |
|--|--------------------|-------------------------------|-----------|-------------------------------|-----------|-------------------------------|-----------|-------------------------------|-----------|------|-------|
|  |                    | Min                           | Max       | Min                           | Max       | Min                           | Max       | Min                           | Max       |      |       |
| <b>Command and Address Timing</b>  |                    |                               |           |                               |           |                               |           |                               |           |      |       |
| DLL locking time   | tDLLK              | 768                           | –         | 1024                          | –         | 1024                          | –         | 1024                          | –         | CK   | 2, 4  |
| CMD, ADDR setup time to CK_t, CK_c Base referenced to V <sub>IH(AC)</sub> and V <sub>IL(AC)</sub> levels | Base               | tIS                           | 62        | –                             | 55        | –                             | 48        | –                             | 40        | –    | ps    |
|  | V <sub>REFCA</sub> | tISVREF                       | 162       | –                             | 145       | –                             | 138       | –                             | 130       | –    | ps    |
| CMD, ADDR hold time to CK_t, CK_c Base referenced to V <sub>IH(DC)</sub> and V <sub>IL(DC)</sub> levels  | Base               | tIH                           | 87        | –                             | 80        | –                             | 73        | –                             | 65        | –    | ps    |
|  | V <sub>REFCA</sub> | tIHVREF                       | 162       | –                             | 145       | –                             | 138       | –                             | 130       | –    | ps    |
| CTRL, ADDR pulse width for each input  | tIPW               | 410                           | –         | 385                           | –         | 365                           | –         | 340                           | –         | ps   |       |
| ACTIVATE to internal READ or WRITE delay   | tRCD               | 14.16                         | –         | 14.25                         | –         | 14.32                         | –         | 13.75                         | –         | ns   |       |
| PRECHARGE command period   | tRP                | 14.16                         | –         | 14.25                         | –         | 14.32                         | –         | 13.75                         | –         | ns   |       |
| ACTIVATE-to-PRECHARGE command period   | tRAS               | 32                            | 9 × tREFI | 32                            | 9 × tREFI | 32                            | 9 × tREFI | 32                            | 9 × tREFI | ns   | 13    |
| ACTIVATE-to-ACTIVATE or REF command period   | tRC                | 46.16                         | –         | 46.25                         | –         | 46.32                         | –         | 45.75                         | –         | ns   | 13    |
| ACTIVATE-to-ACTIVATE command period to different bank groups for 1/2KB page size                         | tRRD_S (1/2KB)     | MIN = greater of 4CK or 3.3ns |           | MIN = greater of 4CK or 3.0ns |           | MIN = greater of 4CK or 2.7ns |           | MIN = greater of 4CK or 2.5ns |           | CK   | 1     |
| ACTIVATE-to-ACTIVATE command period to different bank groups for 1KB page size                           | tRRD_S (1KB)       | MIN = greater of 4CK or 3.3ns |           | MIN = greater of 4CK or 3.0ns |           | MIN = greater of 4CK or 2.7ns |           | MIN = greater of 4CK or 2.5ns |           | CK   | 1     |
| ACTIVATE-to-ACTIVATE command period to different bank groups for 2KB page size                           | tRRD_S (2KB)       | MIN = greater of 4CK or 5.3ns |           | MIN = greater of 4CK or 5.3ns |           | MIN = greater of 4CK or 5.3ns |           | MIN = greater of 4CK or 5.3ns |           | CK   | 1     |
| ACTIVATE-to-ACTIVATE command period to same bank groups for 1/2KB page size                              | tRRD_L (1/2KB)     | MIN = greater of 4CK or 4.9ns |           | MIN = greater of 4CK or 4.9ns |           | MIN = greater of 4CK or 4.9ns |           | MIN = greater of 4CK or 4.9ns |           | CK   | 1     |

| Parameter  | Symbol         | DDR4-2400                                 |                               | DDR4-2666                         |                               | DDR4-2933                     |                               | DDR4-3200 |          | Unit | Notes |
|--|----------------|---|-------------------------------|-----------------------------------|-------------------------------|-------------------------------|-------------------------------|-----------|----------|------|-------|
|  |                | Min                                       | Max                           | Min                               | Max                           | Min                           | Max                           | Min       | Max      |      |       |
| <b>Command and Address Timing</b>  |                |   |                               |                                   |                               |                               |                               |           |          |      |       |
| ACTIVATE-to-ACTIVATE command period to same bank groups for 1KB page size  | tRRD_L (1KB)   | MIN = greater of 4CK or 4.9ns             | MIN = greater of 4CK or 4.9ns | MIN = greater of 4CK or 4.9ns     | MIN = greater of 4CK or 4.9ns | MIN = greater of 4CK or 4.9ns | MIN = greater of 4CK or 4.9ns | CK        | 1        |      |       |
| ACTIVATE-to-ACTIVATE command period to same bank groups for 2KB page size  | tRRD_L (2KB)   | MIN = greater of 4CK or 6.4ns             | MIN = greater of 4CK or 6.4ns | MIN = greater of 4CK or 6.4ns     | MIN = greater of 4CK or 6.4ns | MIN = greater of 4CK or 6.4ns | MIN = greater of 4CK or 6.4ns | CK        | 1        |      |       |
| Four ACTIVATE windows for 1/2KB page size  | tFAW (1/2KB)   | MIN = greater of 16CK or 13ns             | MIN = greater of 16CK or 12ns | MIN = greater of 16CK or 10.875ns | MIN = greater of 16CK or 10ns |                               |                               | ns        |          |      |       |
| Four ACTIVATE windows for 1KB page size  | tFAW (1KB)     | MIN = greater of 20CK or 21ns             | MIN = greater of 20CK or 21ns | MIN = greater of 20CK or 21ns     | MIN = greater of 20CK or 21ns |                               |                               | ns        |          |      |       |
| Four ACTIVATE windows for 2KB page size  | tFAW (2KB)     | MIN = greater of 28CK or 30ns             | MIN = greater of 28CK or 30ns | MIN = greater of 28CK or 30ns     | MIN = greater of 28CK or 30ns |                               |                               | ns        |          |      |       |
| <b>Command and Address Timing</b>  |                |   |                               |                                   |                               |                               |                               |           |          |      |       |
| WRITE recovery time  | tWR            | MIN = 15ns                                |                               |                                   |                               |                               |                               | ns        | 5, 10, 1 |      |       |
|  | tWR2           | MIN = 1CK + tWR                           |                               |                                   |                               |                               |                               | CK        | 5, 11, 1 |      |       |
| WRITE recovery time when CRC and DM are both enabled   | tWR_CRC_DM     | MIN = tWR + greater of (5CK or 3.75ns)    |                               |                                   |                               |                               |                               | CK        | 6, 10, 1 |      |       |
|  | tWR_CRC_DM2    | MIN = 1CK + tWR_CRC_DM                    |                               |                                   |                               |                               |                               | CK        | 6, 11, 1 |      |       |
| Delay from start of internal WRITE transaction to internal READ command – Same bank group                                  | tWTR_L         | MIN = greater of 4CK or 7.5ns             |                               |                                   |                               |                               |                               | CK        | 5, 10, 1 |      |       |
|  | tWTR_L2        | MIN = 1CK + tWTR_L                        |                               |                                   |                               |                               |                               | CK        | 5, 11, 1 |      |       |
| Delay from start of internal WRITE transaction to internal READ command – Same bank group when CRC and DM are both enabled | tWTR_L_CRC_DM  | MIN = tWTR_L + greater of (5CK or 3.75ns) |                               |                                   |                               |                               |                               | CK        | 6, 10, 1 |      |       |
|  | tWTR_L_CRC_DM2 | MIN = 1CK + tWTR_L_CRC_DM                 |                               |                                   |                               |                               |                               | CK        | 6, 11, 1 |      |       |

| Parameter   | Symbol             | DDR4-2400                                  |     | DDR4-2666                   |     | DDR4-2933                   |     | DDR4-3200                   |     | Unit | Notes          |
|---|--------------------|--|-----|-----------------------------|-----|-----------------------------|-----|-----------------------------|-----|------|----------------|
|   |                    | Min  | Max | Min                         | Max | Min                         | Max | Min                         | Max |      |                |
| <b>Command and Address Timing</b>   |                    |  |     |                             |     |                             |     |                             |     |      |                |
| Delay from start of internal WRITE transaction to internal READ command – Different bank group                                  | tWTR_S             | MIN = greater of (2CK or 2.5ns)            |     |                             |     |                             |     |                             |     | CK   | 5, 7, 8, 10, 1 |
|   | tWTR_S2            | MIN = 1CK + tWTR_S                         |     |                             |     |                             |     |                             |     | CK   | 5, 7, 8, 11, 1 |
| Delay from start of internal WRITE transaction to internal READ command – Different bank group when CRC and DM are both enabled | tWTR_S_CRC_D<br>M  | MIN = tWTR_S + greater of (5CK or 3.75ns)  |     |                             |     |                             |     |                             |     | CK   | 6, 7, 8, 10, 1 |
|   | tWTR_S_CRC_D<br>M2 | MIN = 1CK + tWTR_S_CRC_DM                  |     |                             |     |                             |     |                             |     | CK   | 6, 7, 8, 11, 1 |
| READ-to-PRECHARGE time  | tRTP               | MIN = greater of 4CK or 7.5ns              |     |                             |     |                             |     |                             |     | CK   | 1              |
| CAS_n-to-CAS_n command delay to different bank group  | tCCD_S             | 4  | –   | 4                           | –   | 4                           | –   | 4                           | –   | CK   |                |
| CAS_n-to-CAS_n command delay to samebank group  | tCCD_L             | MIN = greater of 5CK or 5ns                | –   | MIN = greater of 5CK or 5ns | –   | MIN = greater of 5CK or 5ns | –   | MIN = greater of 5CK or 5ns | –   | CK   | 15             |
| Auto precharge write recovery + precharge time  | tDAL (MIN)         | MIN = WR + ROUNDUPtRP/tCK (AVG); MAX = N/A |     |                             |     |                             |     |                             |     | CK   |                |
| <b>MRS Command Timing</b>   |                    |  |     |                             |     |                             |     |                             |     |      |                |
| MRS command cycle time  | tMRD               | 8  | –   | 8                           | –   | 8                           | –   | 8                           | –   | CK   |                |
| MRS command cycle time in PDA mode  | tMRD_PDA           | MIN = greater of (16nCK, 10ns)             |     |                             |     |                             |     |                             |     |      | 1              |
| MRS command cycle time in CAL mode  | tMRD_CAL           | MIN = tMOD + tCAL                          |     |                             |     |                             |     |                             |     | CK   |                |
| MRS command update delay  | tMOD               | MIN = greater of (24nCK, 15ns)             |     |                             |     |                             |     |                             |     | CK   | 1              |
| MRS command update delay in PDA mode  | tMOD_PDA           | MIN = tMOD                                 |     |                             |     |                             |     |                             |     | CK   |                |
| MRS command update delay in CAL mode  | tMOD_CAL           | MIN = tMOD + tCAL CK                       |     |                             |     |                             |     |                             |     | CK   |                |

| Parameter   | Symbol         | DDR4-2400                       |          | DDR4-2666 |          | DDR4-2933 |          | DDR4-3200 |          | Unit | Notes |   |
|---|----------------|---------------------------------|----------|-----------|----------|-----------|----------|-----------|----------|------|-------|---|
|   |                | Min                             | Max      | Min       | Max      | Min       | Max      | Min       | Max      |      |       |   |
| <b>MRS Command Timing</b>   |                |                                 |          |           |          |           |          |           |          |      |       |   |
| MRS command to DQS drive in preamble training                                   | tSDO           | MIN = tMOD + 9ns                |          |           |          |           |          |           |          |      | CK    |   |
| <b>MPR Command Timing</b>   |                |                                 |          |           |          |           |          |           |          |      |       |   |
| Multipurpose register recovery time   | tMPRR          | MIN = 1CK                       |          |           |          |           |          |           |          |      | CK    |   |
| Multipurpose register write recovery time                                       | tWR_MPRR       | MIN = tMOD + AL + PL            |          |           |          |           |          |           |          |      |       |   |
| <b>CRC Error Reporting Timing</b>   |                |                                 |          |           |          |           |          |           |          |      |       |   |
| CRC error to ALERT_n latency  | tCRC_ALERT     | 3                               | 13       | 3         | 13       | 3         | 13       | 3         | 13       | ns   |       |   |
| CRC ALERT_n pulse width   | tCRC_ALERT_PW  | 6                               | 10       | 6         | 10       | 6         | 10       | 6         | 10       | CK   |       |   |
| <b>CA Parity Timing</b>   |                |                                 |          |           |          |           |          |           |          |      |       |   |
| Parity latency  | PL             | 5                               | -        | 5         | -        | 6         | -        | 6         | -        | CK   |       |   |
| Commands uncertain to be executed during this time                              | tPAR_UNKNOWN   | -                               | PL       | -         | PL       | -         | PL       | -         | PL       | CK   |       |   |
| Delay from errant command to ALERT_n assertion                                  | tPAR_ALERT_ON  | -                               | PL + 6ns | -         | PL + 6ns | -         | PL + 6ns | -         | PL + 6ns | CK   |       |   |
| Pulse width of ALERT_n signal when asserted                                     | tPAR_ALERT_PW  | 72                              | 144      | 80        | 160      | 88        | 176      | 96        | 192      | CK   |       |   |
| Time from alert asserted until DES command required in persistent CA paritymode | tPAR_ALERT_RSP | -                               | 64       | -         | 71       | -         | 78       | -         | 85       | CK   |       |   |
| <b>CAL Timing</b>   |                |                                 |          |           |          |           |          |           |          |      |       |   |
| CS_n to command address latency   | tCAL           | 5                               | -        | 5         | -        | 6         | -        | 6         | -        | CK   | 20    |   |
| CS_n to command address latency in gear-down mode                               | tCALg          | N/A                             | -        | 6         | -        | 8         | -        | 8         | -        | CK   |       |   |
| <b>MPSM Timing</b>  |                |                                 |          |           |          |           |          |           |          |      |       |   |
| Command path disable delay upon MPSM entry                                      | tMPED          | MIN = tMOD (MIN) + tCPDED (MIN) |          |           |          |           |          |           |          |      | CK    | 1 |
| Valid clock requirement after MPSM entry  | tCKMPE         | MIN = tMOD (MIN) + tCPDED (MIN) |          |           |          |           |          |           |          |      | CK    | 1 |
| Valid clock requirement before MPSM   | tCKMPX         | MIN = tCKSRX (MIN)              |          |           |          |           |          |           |          |      | CK    | 1 |

| Parameter   | Symbol                       | DDR4-2400                       |               | DDR4-2666 |               | DDR4-2933 |               | DDR4-3200 |               | Unit | Notes |   |
|---|------------------------------|---------------------------------|---------------|-----------|---------------|-----------|---------------|-----------|---------------|------|-------|---|
|   |                              | Min                             | Max           | Min       | Max           | Min       | Max           | Min       | Max           |      |       |   |
| <b>MPSM Timing</b>  |                              |                                 |               |           |               |           |               |           |               |      |       |   |
| Exit MPSM to commands not requiring a locked DLL                          | tXMP                         | tXS (MIN)                       |               |           |               |           |               |           |               | CK   |       |   |
| Exit MPSM to commands requiring a locked DLL                              | tXMPDLL                      | MIN = tXMP (MIN) + tXSDLL (MIN) |               |           |               |           |               |           |               | CK   | 1     |   |
| CS setup time to CKE  | tMPX_S                       | MIN = tIS (MIN) + tIH (MIN)     |               |           |               |           |               |           |               | ns   |       |   |
| CS_n HIGH hold time to CKE rising edge                                    | tMPX_HH                      | MIN = tXP                       |               |           |               |           |               |           |               | ns   |       |   |
| CS_n LOW hold time to CKE rising edge                                     | tMPX_LH                      | 12                              | tXMP<br>-10ns | 12        | tXMP<br>-10ns | 12        | tXMP<br>-10ns | 12        | tXMP<br>-10ns | ns   |       |   |
| <b>Connectivity Test Timing</b>   |                              |                                 |               |           |               |           |               |           |               |      |       |   |
| TEN pin HIGH to CS_n LOW – Enter CT mode                                  | tCT_Enable                   | 200                             | –             | 200       | –             | 200       | –             | 200       | –             | ns   |       |   |
| CS_n LOW and valid input to valid output                                  | tCT_Valid                    | –                               | 200           | –         | 200           | –         | 200           | –         | 200           | ns   |       |   |
| CK_t, CK_c valid and CKE HIGH after TEN goes HIGH                         | tCTCKE_Valid                 | 10                              | –             | 10        | –             | 10        | –             | 10        | –             | ns   |       |   |
| <b>Calibration and VREFDQ Train Timing</b>                                |                              |                                 |               |           |               |           |               |           |               |      |       |   |
| ZQCL command: Long calibration time                                       | POWER-UP and RESET operation | tZQinit                         | 1024          | –         | 1024          | –         | 1024          | –         | 1024          | –    | CK    |   |
|   | Normal operation             | tZQoper                         | 512           | –         | 512           | –         | 512           | –         | 512           | –    | CK    |   |
| ZQCS command: Short calibration time                                      |                              | tZQCS                           | 128           | –         | 128           | –         | 128           | –         | 128           | –    | CK    |   |
| The VREF increment/decrement step time                                    |                              | VREF_time                       | MIN = 150ns   |           |               |           |               |           |               |      |       |   |
| Enter VREFDQ training mode to the first write or VREFDQ MRS command delay |                              | tVREFDQE                        | MIN = 150ns   |           |               |           |               |           |               |      | ns    | 1 |
| Exit VREFDQ training mode to the first WRITE command delay                |                              | tVREFDQX                        | MIN = 150ns   |           |               |           |               |           |               |      | ns    | 1 |

| Parameter   | Symbol           | DDR4-2400                                 |                      | DDR4-2666 |     | DDR4-2933 |     | DDR4-3200 |     | Unit | Notes |       |
|---|------------------|---|----------------------|-----------|-----|-----------|-----|-----------|-----|------|-------|-------|
|   |                  | Min                                       | Max                  | Min       | Max | Min       | Max | Min       | Max |      |       |       |
| <b>Initialization and Reset Timing</b>  |                  |   |                      |           |     |           |     |           |     |      |       |       |
| Exit reset from CKE HIGH to a valid command   | tXPR             | MIN = greater of 5CK or tRFC (MIN) + 10ns |                      |           |     |           |     |           |     | CK   | 1     |       |
| RESET_L pulse low after power stable  | tPW_REST_S       | 1.0                                       | -                    | 1.0       | -   | 1.0       | -   | 1.0       | -   | µs   |       |       |
| RESET_L pulse low at power-up   | PW_REST_L        | 200                                       | -                    | 200       | -   | 200       | -   | 200       | -   | µs   |       |       |
| Begin power supply ramp to power supplies stable  | tVDDPR           | MIN = N/A; MAX = 200                      |                      |           |     |           |     |           |     | ms   |       |       |
| RESET_n LOW to power supplies stable  | tRPS             | MIN = 0; MAX = 0                          |                      |           |     |           |     |           |     | ns   |       |       |
| RESET_n LOW to I/O and RTT High-Z   | tIOZ             | MIN = N/A; MAX = undefined                |                      |           |     |           |     |           |     | ns   |       |       |
| <b>Refresh Timing</b>   |                  |   |                      |           |     |           |     |           |     |      |       |       |
| REFRESH-to-ACTIVATE or REFRESH command period (all bank groups)   | 4Gb              | tRFC1                                     | MIN = 260            |           |     |           |     |           |     |      | ns    | 1, 12 |
|   |                  | tRFC2                                     | MIN = 160            |           |     |           |     |           |     |      | ns    | 1, 12 |
|   |                  | tRFC4                                     | MIN = 110            |           |     |           |     |           |     |      | ns    | 1, 12 |
|   | 8Gb              | tRFC1                                     | MIN = 350            |           |     |           |     |           |     |      | ns    | 1, 12 |
|   |                  | tRFC2                                     | MIN = 260            |           |     |           |     |           |     |      | ns    | 1, 12 |
|   |                  | tRFC4                                     | MIN = 160            |           |     |           |     |           |     |      | ns    | 1, 12 |
|   | 16Gb             | tRFC1                                     | MIN = 550            |           |     |           |     |           |     |      | ns    | 1, 12 |
|   |                  | tRFC2                                     | MIN = 350            |           |     |           |     |           |     |      | ns    | 1, 12 |
|   |                  | tRFC4                                     | MIN = 260            |           |     |           |     |           |     |      | ns    | 1, 12 |
| Average periodic refresh interval   | 0°C ≤ TC ≤ 85°C  | tREFI                                     | MIN = N/A; MAX = 7.8 |           |     |           |     |           |     |      | ns    | 12    |
|   | 85°C < TC ≤ 95°C | tREFI                                     | MIN = N/A; MAX = 3.9 |           |     |           |     |           |     |      | µs    | 12    |
| <b>Self Refresh Timing</b>  |                  |   |                      |           |     |           |     |           |     |      |       |       |
| Exit self refresh to commands not requiring a locked DLL SRX to commands not requiring a locked DLL in self refresh abort | tXS              | MIN = tRFC + 10ns                         |                      |           |     |           |     |           |     | ns   | 1     |       |
|   | tXS_ABORT        | MIN = tRFC4 + 10ns                        |                      |           |     |           |     |           |     | ns   | 1     |       |
| Exit self refresh to ZQCL, ZQCS and MRS (CL, CWL, WR, RTP and gear-down)  | tXS_FAST         | MIN = tRFC4 + 10ns                        |                      |           |     |           |     |           |     | ns   | 1     |       |

| Parameter | Symbol | DDR4-2400 |     | DDR4-2666 |     | DDR4-2933 |     | DDR4-3200 |     | Unit | Notes |
|-----------|--------|-----------|-----|-----------|-----|-----------|-----|-----------|-----|------|-------|
|           |        | Min       | Max | Min       | Max | Min       | Max | Min       | Max |      |       |



| Self Refresh Timing  |            |   |   |   |   |   |   |   |   |    |   |
|--|------------|---|---|---|---|---|---|---|---|----|---|
| Exit self refresh to commands requiring a locked DLL   | tXSDLL     | MIN = tDLLK (MIN)   |   |   |   |   |   |   |   | CK | 1 |
| Minimum CKE low pulse width for self refresh entry to self refresh exit timing                             | tCKESR     | MIN = tCKE (MIN) + 1nCK                                       |   |   |   |   |   |   |   | CK | 1 |
| Minimum CKE low pulse width for self refresh entry to self refresh exit timing when CA parity is enabled   | tCKESR_PAR | MIN = tCKE (MIN) + 1nCK + PL                                  |   |   |   |   |   |   |   | CK | 1 |
| Valid clocks after self refresh entry (SRE) or power-down entry (PDE)                                      | tCKSRE     | MIN = greater of (5CK, 10ns)                                  |   |   |   |   |   |   |   | CK | 1 |
| Valid clock requirement after self refresh entry or power-down when CA parity is enabled                   | tCKSRE_PAR | MIN = greater of (5CK, 10ns) + PL                             |   |   |   |   |   |   |   | CK | 1 |
| Valid clocks before self refresh exit (SRX) or power-down exit (PDX), or reset exit                        | tCKSRX     | MIN = greater of (5CK, 10ns)                                  |   |   |   |   |   |   |   | CK | 1 |
| Power-Down Timing  |            |   |   |   |   |   |   |   |   |    |   |
| Exit power-down with DLL on to any valid command   | tXP        | MIN = greater of 4CK or 6ns                                   |   |   |   |   |   |   |   | CK | 1 |
| Exit precharge power-down with DLL frozen to commands not requiring a locked DLL when CA Parity is enabled | tXP_PAR    | MIN = (greater of 4CK or 6ns) + PL                            |   |   |   |   |   |   |   | CK | 1 |
| CKE MIN pulse width  | tCKE (MIN) | MIN = greater of 3CK or 5ns                                   |   |   |   |   |   |   |   | CK |   |
| Command pass disable delay   | tCPDED     | 4   | - | 4 | - | 4 | - | 4 | - | CK |   |
| Power-down entry to power-down exit timing   | tPD        | MIN = tCKE (MIN); MAX = 9 × tREFI                             |   |   |   |   |   |   |   | CK |   |
| Begin power-down period prior to CKE registered HIGH   | tANPD      | WL - 1CK  |   |   |   |   |   |   |   | CK |   |
| Power-down entry period: ODT either synchronous or asynchronous  | PDE        | Greater of tANPD or tRFC - REFRESH command to CKE<br>LOW time |   |   |   |   |   |   |   | CK |   |

| Parameter | Symbol | DDR4-2400 |     | DDR4-2666 |     | DDR4-2933 |     | DDR4-3200 |     | Unit | Notes |
|-----------|--------|-----------|-----|-----------|-----|-----------|-----|-----------|-----|------|-------|
|           |        | Min       | Max | Min       | Max | Min       | Max | Min       | Max |      |       |
|           |        |           |     |           |     |           |     |           |     |      |       |

| Power-Down Timing  |             |                              |     |      |      |      |      |      |      |    |   |
|--|-------------|------------------------------|-----|------|------|------|------|------|------|----|---|
| Power-down exit period: ODT either synchronous or asynchronous               | PDX         | tANPD + tXSDLL               |     |      |      |      |      |      |      | CK |   |
| Power-Down Entry Minimum Timing  |             |                              |     |      |      |      |      |      |      |    |   |
| ACTIVATE command to power-down entry   | tACTPDEN    | 2                            | -   | 2    | -    | 2    | -    | 2    | -    | CK |   |
| PRECHARGE/PRECHARGE ALL command to power-down entry                          | tPRPDEN     | 2                            | -   | 2    | -    | 2    | -    | 2    | -    | CK |   |
| REFRESH command to power-down entry  | tREFPDEN    | 2                            | -   | 2    | -    | 2    | -    | 2    | -    | CK |   |
| MRS command to power-down entry  | tMRSPDEN    | MIN = tMOD (MIN)             |     |      |      |      |      |      |      | CK | 1 |
| READ/READ with auto precharge command to power-down entry                    | tRDPDEN     | MIN = RL + 4 + 1             |     |      |      |      |      |      |      | CK | 1 |
| WRITE command to power-down entry (BL8OTF, BL8MRS, BC4OTF)                   | tWRPDEN     | MIN = WL + 4 + tWR/tCK (AVG) |     |      |      |      |      |      |      | CK | 1 |
| WRITE command to power-down entry(BC4MRS)                                    | tWRPBC4DEN  | MIN = WL + 2 + tWR/tCK (AVG) |     |      |      |      |      |      |      | CK | 1 |
| WRITE with auto precharge command to power-down entry (BL8OTF,BL8MRS,BC4OTF) | tWRAPDEN    | MIN = WL + 4 + WR + 1        |     |      |      |      |      |      |      | CK | 1 |
| WRITE with auto precharge command to power-down entry (BC4MRS)               | tWRAPBC4DEN | MIN = WL + 2 + WR + 1        |     |      |      |      |      |      |      | CK | 1 |
| ODT Timing   |             |                              |     |      |      |      |      |      |      |    |   |
| Direct ODT turn-on latency   | DODTLon     | WL - 2 = CWL + AL + PL - 2   |     |      |      |      |      |      |      | CK |   |
| Direct ODT turn-off latency  | DODTLoff    | WL - 2 = CWL + AL + PL - 2   |     |      |      |      |      |      |      | CK |   |
| R <sub>TT</sub> dynamic change skew  | tADC        | 0.3                          | 0.7 | 0.28 | 0.72 | 0.26 | 0.74 | 0.26 | 0.74 | CK |   |
| Asynchronous RTT(NOM) turn-on delay (DLL off)                                | tAONAS      | 1                            | 9   | 1    | 9    | 1    | 9    | 1    | 9    | ns |   |
| Asynchronous RTT(NOM) turn-off delay (DLL off)                               | tAOFAS      | 1                            | 9   | 1    | 9    | 1    | 9    | 1    | 9    | ns |   |

| Parameter | Symbol | DDR4-2400 |     | DDR4-2666 |     | DDR4-2933 |     | DDR4-3200 |     | Unit | Notes |
|-----------|--------|-----------|-----|-----------|-----|-----------|-----|-----------|-----|------|-------|
|           |        | Min       | Max | Min       | Max | Min       | Max | Min       | Max |      |       |

| ODT Timing   |             |      |     |            |     |            |     |            |     |           |  |
|--|-------------|------|-----|------------|-----|------------|-----|------------|-----|-----------|--|
| ODT HIGH time with WRITE command and BL8   | ODTH8 1'CK  | 6    | –   | 6          | –   | 6          | –   | 6          | –   | CK        |  |
|  | ODTH8 2'CK  | 7    | –   | 7          | –   | 7          | –   | 7          | –   |           |  |
| ODT HIGH time without WRITE command or with WRITE command and BC4                    | ODTH4 1'CK  | 4    | –   | 4          | –   | 4          | –   | 4          | –   | CK        |  |
|  | ODTH4 2'CK  | 5    | –   | 5          | –   | 5          | –   | 5          | –   |           |  |
| Write Leveling Timing  |             |      |     |            |     |            |     |            |     |           |  |
| First DQS_t, DQS_c rising edge after write leveling mode is programmed               | tWLMRD      | 40   | –   | 40         | –   | 40         | –   | 40         | –   | CK        |  |
| DQS_t, DQS_c delay after write leveling mode is programmed                           | tWLDQSEN    | 25   | –   | 25         | –   | 25         | –   | 25         | –   | CK        |  |
| Write leveling setup from rising CK_t, CK_c crossing to rising DQS_t, DQS_c crossing | tWLS        | 0.13 | –   | 0.13       | –   | 0.13       | –   | 0.13       | –   | tCK (AVG) |  |
| Write leveling hold from rising DQS_t, DQS_c crossing to rising CK_t, CK_c crossing  | tWLH        | 0.13 | –   | 0.13       | –   | 0.13       | –   | 0.13       | –   | tCK (AVG) |  |
| Write leveling output delay  | tWLO        | 0    | 9.5 | 0          | 9.5 | 0          | 9.5 | 0          | 9.5 | ns        |  |
| Write leveling output error  | tWLOE       | 0    | 2   | 0          | 2   | 0          | 2   | 0          | 2   | ns        |  |
| Gear-Down Timing (Not Supported Below DDR4-2666)                                     |             |      |     |            |     |            |     |            |     |           |  |
| Exit reset from CKE HIGH to a valid MRS gear-down                                    | tXPR_GEAR   | N/A  |     | tXPR       |     | tXPR       |     | tXPR       |     | CK        |  |
| CKE HIGH assert to gear-down enable time   | tXS_GEAR    | N/A  |     | tXS        |     | tXS        |     | tXS        |     | CK        |  |
| MRS command to sync pulse time   | tSYNC_GEAR  | N/A  |     | tMOD + 4CK |     | tMOD + 4CK |     | tMOD + 4CK |     | CK        |  |
| Sync pulse to first valid command  | tCMD_GEAR   | N/A  |     | tMOD       |     | tMOD       |     | tMOD       |     | CK        |  |
| Gear-down setup time   | tGEAR_setup | N/A  | –   | 2CK        | –   | 2CK        | –   | 2CK        | –   | CK        |  |
| Gear-down hold time  | tGEAR_hold  | N/A  | –   | 2CK        | –   | 2CK        | –   | 2CK        | –   | CK        |  |

NOTES :

1. Maximum limit not applicable.

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2. tCCD\_L and tDLLK should be programmed according to the value defined per operating frequency.
  3. Data rate is greater than or equal to 1066 Mb/s.
  4. RFU.
  5. WRITE-to-READ when CRC and DM are both not enabled.
  6. WRITE-to-READ delay when CRC and DM are both enabled.
  7. The start of internal write transactions is defined as follows:
    - For BL8 (fixed by MRS and on-the-fly): rising clock edge four clock cycles after WL
    - For BC4 (on-the-fly): rising clock edge four clock cycles after WL
    - For BC4 (fixed by MRS): rising clock edge two clock cycles after WL
  8. For these parameters, the device supports  $t_{nPARAM} [nCK] = RU\{t_{PARAM} [ns]/t_{CK} (AVG) [ns]\}$ , in clock cycles, assuming all input clock jitter specifications are satisfied.
  9. Although unlimited row accesses to the same row is allowed within the refresh period, excessive row accesses to the same row over a long term can result in degraded operation.
  10. When operating in 1tCK WRITE preamble mode.
  11. When operating in 2tCK WRITE preamble mode.
  12. When CA parity mode is selected and the DLLoff mode is used, each REF command requires an additional "PL" added to tRFC refresh time.
  13. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in reduction of the product lifetime and/or reduction in data retention ability.
  14. Applicable from tCK (AVG) MIN to tCK (AVG) MAX as stated in the Speed Bin tables.
  15. JEDEC specifies a minimum of five clocks.
  16. The maximum read postamble is bound by tDQSCK (MIN) plus tQSH (MIN) on the left side and tHZ(DQS) MAX on the right side.
  17. The reference level of DQ output signal is specified with a midpoint as a widest part of output signal eye, which should be approximately  $0.7 \times V_{DDQ}$  as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to  $V_{TT} = V_{DDQ}$ .
  18. JEDEC hasn't agreed upon the definition of the deterministic jitter; the user should focus on meeting the total limit.
  19. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread-spectrum at a sweep rate in the range of 20–60 kHz with an additional 1% of tCK (AVG) as a long-term jitter component; however, the spread spectrum may not use a clock rate below tCK (AVG) MIN.
  20. The actual tCAL minimum is the larger of 3 clocks or 3.748ns/tCK; the table lists the applicable clocks required at targeted speed bin.
  21. The maximum READ preamble is bounded by tLZ(DQS) MIN on the left side and tDQSCK (MAX) on the right side. See figure in Clock to Data Strobe Relationship. Boundary of DQS Low-Z occur one cycle earlier in 2tCK toggle mode which is illustrated in READ Preamble.
  22. DQ falling signal middle-point of transferring from HIGH to LOW to first rising edge of DQS differential signal cross-point.
    23. The tPDA\_S/tPDA\_H parameters may use the tDS/tDH limits, respectively, if the signal is LOW the entire BL8
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**SERIAL PRESENCE DETECT SPECIFICATION (AQD-D4U16GN32-SE Serial Presence Detect)**

| Byte  | Function Described   | Function                                 | HEX Value |
|-------|--|--|-----------|
| 0     | Number of Bytes Used / Number of Bytes in SPD Device / CRC Coverage          | SPD Total: 512Bytes, SPD Used : 384Bytes | 23        |
| 1     | SPD Revision   | Version 1.1                              | 11        |
| 2     | Key Byte / DRAM Device Type  | DDR4 SDRAM                               | 0C        |
| 3     | Key Byte / Module Type   | U-DIMM                                   | 02        |
| 4     | SDRAM Density and Banks  | 4 bank group / 4 bank      8Gb           | 85        |
| 5     | SDRAM Addressing   | Row : 16      Column : 10                | 21        |
| 6     | SDRAM Package Type   | Mono / Not specified                     | 00        |
| 7     | SDRAM Optional Features  | Unlimited MAC                            | 08        |
| 8     | SDRAM Thermal and Refresh Options  | -  | 00        |
| 9     | Other SDRAM Optional Features  | hPPR,sPPR supported                      | 60        |
| 10    | Reserved   | -  | 00        |
| 11    | Module Nominal Voltage, VDD  | 1.2v                                     | 03        |
| 12    | Module Organization  | 2Rank      x8                            | 09        |
| 13    | Module Memory Bus Width  | Non ECC      64bits                      | 03        |
| 14    | Module Thermal Sensor  | Non Thermal Sensor                       | 00        |
| 15-16 | Reserved   | -  | 00        |
| 17    | Timebases  | MTB: 125ps      FTB: 1ps                 | 00        |
| 18    | SDRAM Minimum Cycle Time (tCKAVGmin)   | 0.625 ns                                 | 05        |
| 19    | SDRAM Maximum Cycle Time (tCKAVGmax)   | 1.6 ns                                   | 0D        |
| 20    | CAS Latencies Supported, First Byte  | CL 10,11,12,13,14                        | F8        |
| 21    | CAS Latencies Supported, Second Byte   | CL 15,16,17,18,19,20,22                  | BF        |
| 22    | CAS Latencies Supported, Third Byte  | CL24                                     | 02        |
| 23    | CAS Latencies Supported, Fourth Byte   | -  | 00        |
| 24    | Minimum CAS Latency Time(tAAMin)   | 13.75 ns                                 | 6E        |
| 25    | Minimum RAS to CAS Delay Time (tRCDmin)                                      | 13.75 ns                                 | 6E        |
| 26    | Minimum Row Precharge Delay Time (tRPmin)                                    | 13.75 ns                                 | 6E        |
| 27    | Upper Nibbles for tRASmin and tRCmin   | -  | 11        |
| 28    | Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte     | 32 ns                                    | 00        |
| 29    | Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte | 45.75 ns                                 | 6E        |
| 30    | Minimum Refresh Recovery Delay Time (tRFC1min), Least Significant Byte       | -  | F0        |
| 31    | Minimum Refresh Recovery Delay Time (tRFC1min), Most Significant Byte        | 350 ns                                   | 0A        |
| 32    | Minimum Refresh Recovery Delay Time (tRFC2min), Least Significant Byte       | -  | 20        |
| 33    | Minimum Refresh Recovery Delay Time (tRFC2min), Most Significant Byte        | 260 ns                                   | 08        |
| 34    | Minimum Refresh Recovery Delay Time (tRFC4min), Least Significant Byte       | -  | 00        |
| 35    | Minimum Refresh Recovery Delay Time (tRFC4min), Most Significant Byte        | 160 ns                                   | 05        |
| 36    | Minimum Four Activate Window Time (tFAWmin), Most Significant Nibble         | 21 ns                                    | 00        |
| 37    | Minimum Four Activate Window Time (tFAWmin), Least Significant Byte          | -  | A8        |
| 38    | Minimum Activate to Activate Delay Time (tRRD_Smin), different bank group    | 2.5 ns                                   | 14        |
| 39    | Minimum Activate to Activate Delay Time (tRRD_Lmin), same bank group         | 4.9 ns                                   | 28        |
| 40    | Minimum CAS to CAS Delay Time (tCCD_Lmin), same bank group                   | 5 ns                                     | 28        |
| 41    | Upper Nibble for tWRmin  | 15 ns                                    | 00        |
| 42    | Minimum Write Recovery Time(tWRmin)  | 15 ns                                    | 78        |
| 43    | Upper Nibbles for tWTRmin  | 2.5/7.5 ns                               | 00        |
| 44    | Minimum Write to Read Time(tWTR_Smin) , different bank group                 | 2.5 ns                                   | 14        |
| 45    | Minimum Write to Read Time(tWTR_Lmin) , same bank group                      | 7.5 ns                                   | 3C        |
| 46-59 | Reserved, Base Configuration Section   | -  | 00        |
| 60    | Connector to SDRAM Bit Mapping   | DQ0, DQ1, DQ2, DQ3                       | 15        |
| 61    | Connector to SDRAM Bit Mapping   | DQ4, DQ5, DQ6, DQ7                       | 2B        |
| 62    | Connector to SDRAM Bit Mapping   | DQ8, DQ9, DQ10, DQ11                     | 16        |
| 63    | Connector to SDRAM Bit Mapping   | DQ12, DQ13, DQ14, DQ15                   | 36        |
| 64    | Connector to SDRAM Bit Mapping   | DQ16, DQ17, DQ18, DQ19                   | 0B        |
| 65    | Connector to SDRAM Bit Mapping   | DQ20, DQ21, DQ22, DQ23                   | 2B        |
| 66    | Connector to SDRAM Bit Mapping   | DQ24, DQ25, DQ26, DQ27                   | 0C        |
| 67    | Connector to SDRAM Bit Mapping   | DQ28, DQ29, DQ30, DQ31                   | 36        |
| 68    | Connector to SDRAM Bit Mapping   | CB0-3                                    | 00        |
| 69    | Connector to SDRAM Bit Mapping   | CB4-7                                    | 00        |
| 70    | Connector to SDRAM Bit Mapping   | DQ32, DQ33, DQ34, DQ35                   | 36        |
| 71    | Connector to SDRAM Bit Mapping   | DQ36, DQ37, DQ38, DQ39                   | 15        |
| 72    | Connector to SDRAM Bit Mapping   | DQ40, DQ41, DQ42, DQ43                   | 2B        |
| 73    | Connector to SDRAM Bit Mapping   | DQ44, DQ45, DQ46, DQ47                   | 0C        |
| 74    | Connector to SDRAM Bit Mapping   | DQ48, DQ49, DQ50, DQ51                   | 2C        |
| 75    | Connector to SDRAM Bit Mapping   | DQ52, DQ53, DQ54, DQ55                   | 16        |
| 76    | Connector to SDRAM Bit Mapping   | DQ56, DQ57, DQ58, DQ59                   | 2B        |

| Byte    | Function Described   | Function                | HEX Value |
|---------|--|-------------------------|-----------|
| 77      | Connector to SDRAM Bit Mapping   | DQ60, DQ61, DQ62, DQ63  | 0C        |
| 78~116  | Reserved, Base Configuration Section   | -                       | 00        |
| 117     | Fine Offset for Minimum CAS to CAS Delay Time(tCCD_Lmin), same bank group                | 0ns                     | 00        |
| 118     | Fine Offset for Minimum Activate to Activate Delay Time(tRRD_Lmin), different bank group | -0.1ns                  | 9C        |
| 119     | Fine Offset for Minimum Activate to Activate Delay Time(tRRD_Smin), same bank group      | 0ns                     | 00        |
| 120     | Fine Offset for Minimum Activate to Activate/Refresh Delay Time(tRCmin)                  | 0ns                     | 00        |
| 121     | Fine Offset for Minimum Row Precharge Delay Time(tRPmin)                                 | 0ns                     | 00        |
| 122     | Fine Offset for Minimum RAS to CAS Delay Time(tRCDmin)                                   | 0ns                     | 00        |
| 123     | Fine Offset for Minimum CAS Latency Time(tAmin)  | 0ns                     | 00        |
| 124     | Fine Offset for SDRAM Maximum Cycle Time(tCKAVGmax)                                      | -0.025ns                | E7        |
| 125     | Fine Offset for SDRAM Minimum Cycle Time(tCKAVGmin)                                      | 0ns                     | 00        |
| 126     | Cyclical Redundancy Code for Base Configuration Section, LSB                             | CRC-CCITT(LOW)          | 88        |
| 127     | Cyclical Redundancy Code for Base Configuration Section, MSB                             | CRC-CCITT(HIGH)         | C7        |
| 128     | (Unbuffered): Raw Card Extension, Module Nominal Height                                  | Revision 2   31.25 mm   | 11        |
| 129     | (Unbuffered): Module Maximum Thickness   | -                       | 11        |
| 130     | (Unbuffered): Reference Raw Card Used  | Raw Card B   Revision 2 | 41        |
| 131     | (Unbuffered): Address Mapping from Edge Connector to DRAM                                | Mirrored                | 01        |
| 132~253 | (Unbuffered): Reserved   | -                       | 00        |
| 254     | (Unbuffered): CRC for Module Specific Section, Least Significant Byte                    | CRC-CCITT(LOW)          | AB        |
| 255     | (Unbuffered): CRC for Module Specific Section, Most Significant Byte                     | CRC-CCITT(HIGH)         | C6        |
| 256~319 | Hybrid Memory Architecture Specific Parameters   |                         | 00        |
| 320     | Module Manufacturer ID Code, LSB   |                         | 04        |
| 321     | Module Manufacturer ID Code, MSB   |                         | CB        |
| 322     | Module ID: Module Manufacturing Location   | *Note: 1                | -         |
| 323     | Module ID: Module Manufacturing Date(Year)   | *Note: 2                | -         |
| 324     | Module ID: Module Manufacturing Date(Week)   | *Note: 3                | -         |
| 325~328 | Module ID : Module Serial Number   | *Note: 4                | -         |
| 329~348 | Module Part Number   | *Note: 5                | -         |
| 349     | Module Revision Code   | -                       | 00        |
| 350     | SDRAM Manufacturer's JEDEC ID Code, LSB  | Samsung                 | 80        |
| 351     | SDRAM Manufacturer's JEDEC ID Code, MSB  |                         | CE        |
| 352     | DRAM Stepping  | -                       | FF        |
| 353~381 | Manufacturer's Specific Data   | *Note: 7                | -         |
| 382     | Reserved   |                         | 00        |
| 383     | Reserved   |                         | 00        |
| 384~511 | End User Programmable  | *Note: 8                | -         |

- Note :
1. Byte 322 -- Manufacturing location by manufacturing location (00:Taiwan /01:China)
  2. Byte 323 -- Module manufacturing date by year (YY).
  3. Byte 324 -- Module manufacturing date by week (WW).
  4. Bytes 325~328 -- Module Serial Number.
  5. Bytes 329~348 -- Manufacturer Part Number by module part number , (Unused digits are coded as ASCII blanks (20h)).
  6. Bytes 353~381 -- These bytes are undefined and can be used own purpose. Digits are coded as 00h except the following:
    - 6-1. Bytes 353~367 -- Manufacturer's Specific Data by working order number.
    - 6-2. Bytes 368~381 -- Manufacturer's Specific Data by SPD naming number.
  7. Bytes 384~511 -- These bytes are undefined and can be used own purpose. Digits are coded as 00h except the following:
    - 7-1. Bytes 384 -- The byte is coded as ADh.