Advantech

AQD-D5V16GR48-SB
Datasheet

Rev. 1.0

2022-05-23

Description

AQD-D5V16GR48-SB is DDR5-4800(CL40)-39-39 SDRAM memory module. The SPD is programmed to JEDEC standard latency 4800Mbps timing of 40-39-39 at 1.1V. The module is composed of 16Gb CMOS DDR5 SDRAMs in FBGA package and one 8Kbit SPD Hub in 8pin TDFN package on a 288pin glass–epoxy printed circuit board.

The module is a Dual In-line Memory Module and intended for mounting onto 288 pins edge connector sockets. Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

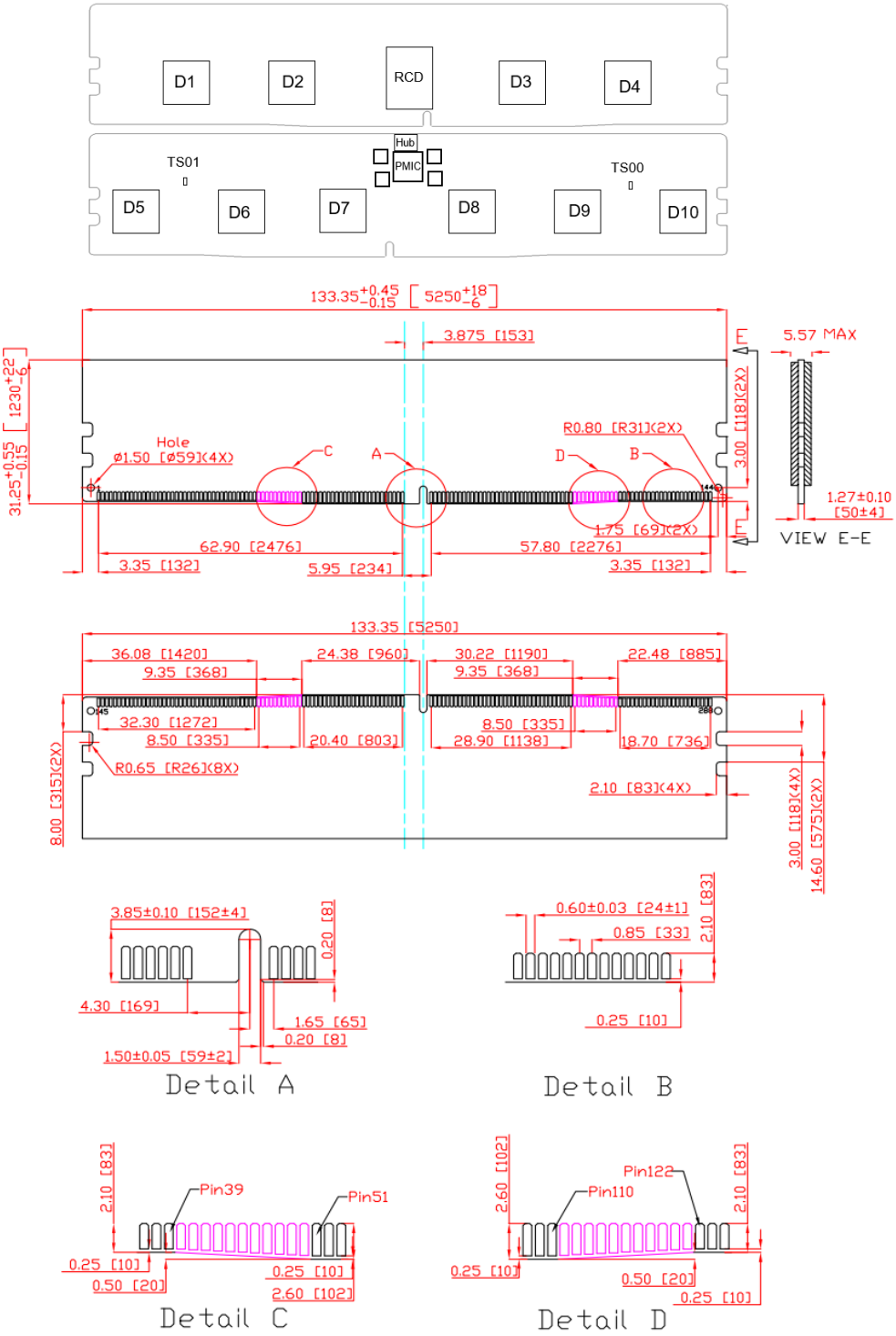
- RoHS compliant products.
- JEDEC standard 1.1V(1.067V~1.166V) Power supply
- VDDQ= 1.1V(1.067V~1.166V)
- VPP = 1.8V(+0.108V / -0.054V)
- Data transfer rates: PC5-4800
- Programmable CAS Latency:22,26,28,30,32,36,40,42
- 16 bit pre-fetch
- Burst Length (BL) switch on-the-fly BL16 or BC8
- Bi-directional Differential Data-Strobe
- On Die Termination, Nominal, Park
- Serial presence detect hub (SPD Hub) with Integrated Temperature sensor
- Asynchronous reset
- PCB edge connector treated with 30u” Gold-Plating

Pin Descriptions

Pin Name	Description		Pin Name	Description
CA[6:0]_A CA[6:0]_B	Address and Command Bus		DQ[31:0]_A DQ[31:0]_B	DIMM memory Data bus channel A & B
CS[1:0]_A CS[1:0]_B	Chip Select		CB[7:0]_A CB[7:0]_B	DIMM ECC Checkbits (CB) channel A & B
PAR_A PAR_B	Parity input		DQS[9:0]_A_t DQS[9:0]_B_t	Data Strobes (positive line of differential pair)
CK_t	Clocks (true/positive)		DQS[9:0]_A_c DQS[9:0]_B_c	Data Strobes (negative line of differential pair)
CK_c	Clocks (complement/negative)		TDQS[9:5]_A_t TDQS[9:5]_B_t	Not valid for x4 operation. Enabled via Mode Register.
ALERT_n	Alert for CRC error		TDQS[9:5]_A_c TDQS[9:5]_B_c	Not valid for x4 operation. Enabled via Mode Register.
RESET_n	Set DRAM to known state		VIN_BULK	DIMM Power Supply from system to PMIC
PCAMP	Control and Monitor Port		VIN_MGMT	DIMM Power Supply from system to PMIC
HSCL	I2C/I3C-Basic Host Sideband Bus Clock		VSS	Power supply return (ground)
HSDA	I2C/I3C-Basic Host Sideband Bus Data		RFU	Reserved for future use
HSA	I2C/I3C-Basic Host Sideband Bus Address		LBDQS	Loopback Data strobe output
LBDQ	Loopback Data output:			

1. TDQSx and DQSx_t share a pin..

Dimensions (Unit: millimeter)



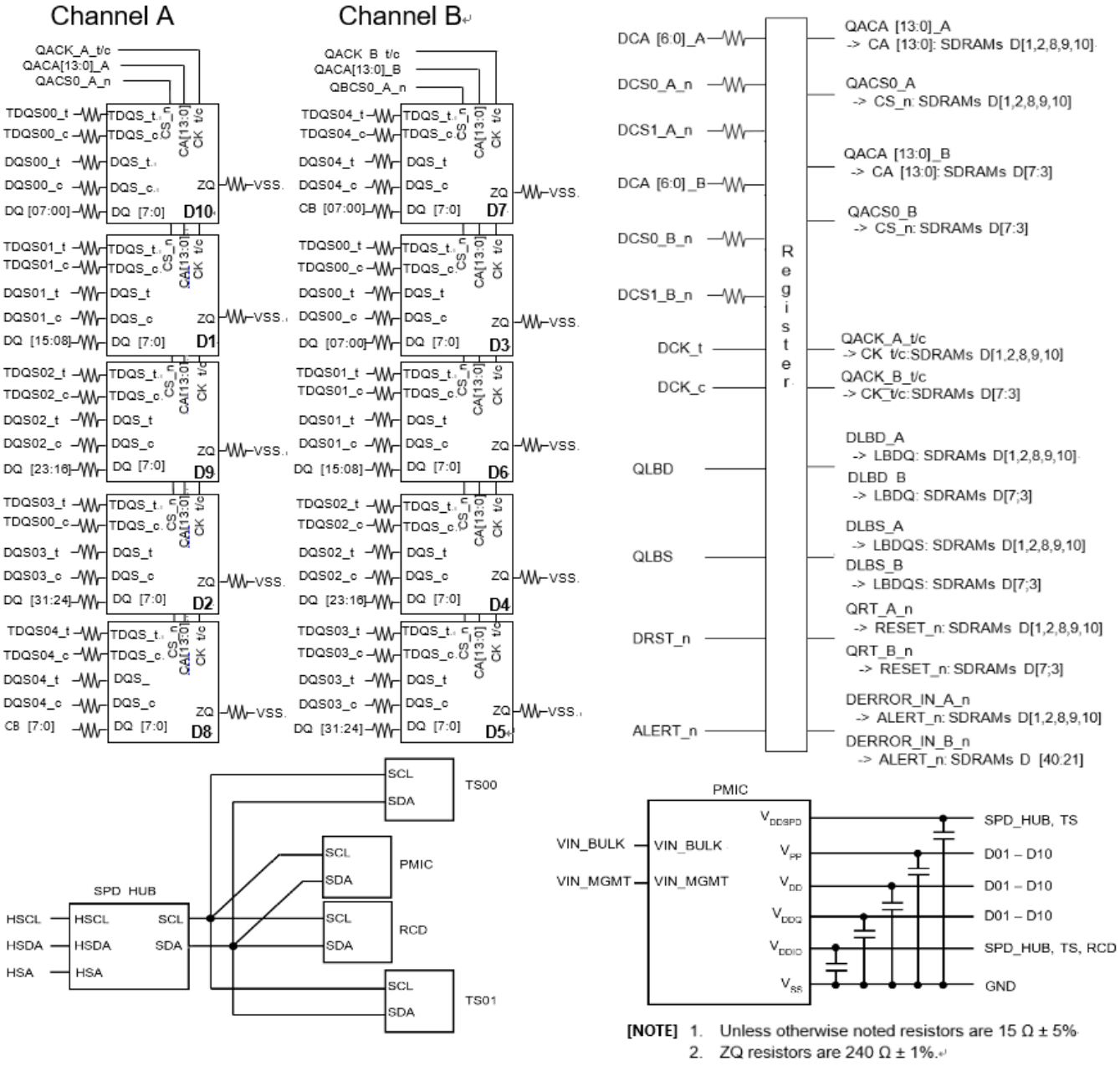
Note:1. Tolerances on all dimensions +/-0.15mm unless otherwise specified.

Pin Assignments

DDR5 288Pin R-DIMM											
Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VIN_BULK	50	VSS	96	CB0_B	145	VIN_BULK	194	DQ31_A	240	VSS
2	RFU	51	CB0_A	97	VSS	146	VIN_BULK	195	VSS	241	CB2_B
3	VIN_MGMT	52	VSS	98	CB1_B	147	PCAMP	196	CB2_A	242	VSS
4	HSCL	53	CB1_A	99	VSS	148	HSA	197	VSS	243	CB3_B
5	HSDA	54	VSS	100	DQ0_B	149	RFU	198	CB3_A	244	VSS
6	VSS	55	DQS4_A_t	101	VSS	150	RFU	199	VSS	245	DQ2_B
7	DQ0_A	56	DQS4_A_c	102	DQ1_B	151	VSS	200	DQS9_A_c, TDQS9_A_c	246	VSS
8	VSS	57	VSS	103	VSS	152	DQ2_A	201	DQS9_A_t, TDQS9_A_t	247	DQ3_B
9	DQ1_A	58	CB4_A	104	DQS0_B_t	153	VSS	202	VSS	248	VSS
10	VSS	59	VSS	105	DQS0_B_c	154	DQ3_A	203	CB6_A	249	DQS5_B_c, TDQS5_B_c
11	DQS0_A_t	60	CB5_A	106	VSS	155	VSS	204	VSS	250	DQS5_B_t, TDQS5_B_t
12	DQS0_A_c	61	VSS	107	DQ4_B	156	DQS5_A_c, TDQS5_A_c	205	CB7_A	251	VSS
13	VSS	62	ALERT_n	108	VSS	157	DQS5_A_t, TDQS5_A_t	206	VSS	252	DQ6_B
14	DQ4_A	63	VSS	109	DQ5_B	158	VSS	207	RESET_n	253	VSS
15	VSS	64	CS0_A_n	110	VSS	159	DQ6_A	208	VSS	254	DQ7_B
16	DQ5_A	65	VSS	111	DQ8_B	160	VSS	209	CS1_A_n	255	VSS
17	VSS	66	CA0_A	112	VSS	161	DQ7_A	210	VSS	256	DQ10_B
18	DQ8_A	67	VSS	113	DQ9_B	162	VSS	211	CA1_A	257	VSS
19	VSS	68	CA2_A	114	VSS	163	DQ10_A	212	VSS	258	DQ11_B
20	DQ9_A	69	VSS	115	DQS1_B_t	164	VSS	213	CA3_A	259	VSS
21	VSS	70	CA4_A	116	DQS1_B_c	165	DQ11_A	214	VSS	260	DQS6_B_c, TDQS6_B_c
22	DQS1_A_t	71	VSS	117	VSS	166	VSS	215	CA5_A	261	DQS6_B_t, TDQS6_B_t
23	DQS1_A_c	72	CA6_A	118	DQ12_B	167	DQS6_A_c, TDQS6_A_c	216	VSS	262	VSS
24	VSS	73	VSS	119	VSS	168	DQS6_A_t, TDQS6_A_t	217	CK_t	263	DQ14_B
25	DQ12_A	74	PAR_A	120	DQ13_B	169	VSS	218	CK_c	264	VSS
26	VSS	75	VSS	121	VSS	170	DQ14_A	219	VSS	265	DQ15_B
27	DQ13_A	Key		122	DQ16_B	171	VSS	Key		266	VSS
28	VSS			123	VSS	172	DQ15_A			267	DQ18_B
29	DQ16_A			124	DQ17_B	173	VSS			268	VSS
30	VSS	76	CA0_B	125	VSS	174	DQ18_A	220	RFU	269	DQ19_B
31	DQ17_A	77	VSS	126	DQS2_B_t	175	VSS	221	CA1_B	270	VSS
32	VSS	78	CA2_B	127	DQS2_B_c	176	DQ19_A	222	VSS	271	DQS7_B_c, TDQS7_B_c
33	DQS2_A_t	79	VSS	128	VSS	177	VSS	223	CA3_B	272	DQS7_B_t, TDQS7_B_t
34	DQS2_A_c	80	CA4_B	129	DQ20_B	178	DQS7_A_c, TDQS7_A_c	224	VSS	273	VSS
35	VSS	81	VSS	130	VSS	179	DQS7_A_t, TDQS7_A_t	225	CA5_B	274	DQ22_B
36	DQ20_A	82	CA6_B	131	DQ21_B	180	VSS	226	VSS	275	VSS
37	VSS	83	VSS	132	VSS	181	DQ22_A	227	PAR_B	276	DQ23_B
38	DQ21_A	84	CS0_B_n	133	DQ24_B	182	VSS	228	VSS	277	VSS
39	VSS	85	VSS	134	VSS	183	DQ23_A	229	CS1_B_n	278	DQ26_B
40	DQ24_A	86	DLBDQ	135	DQ25_B	184	VSS	230	VSS	279	VSS
41	VSS	87	DLBDQS	136	VSS	185	DQ26_A	231	RFU	280	DQ27_B
42	DQ25_A	88	VSS	137	DQS3_B_t	186	VSS	232	RFU	281	VSS
43	VSS	89	CB4_B	138	DQS3_B_c	187	DQ27_A	233	VSS	282	DQS8_B_c, TDQS8_B_c
44	DQS3_A_t	90	VSS	139	VSS	188	VSS	234	CB6_B	283	DQS8_B_t, TDQS8_B_t
45	DQS3_A_c	91	CB5_B	140	DQ28_B	189	DQS8_A_c, TDQS8_A_c	235	VSS	284	VSS
46	VSS	92	VSS	141	VSS	190	DQS8_A_t, TDQS8_A_t	236	CB7_B	285	DQ30_B
47	DQ28_A	93	DQS9_B_t, TDQS9_B_t	142	DQ29_B	191	VSS	237	VSS	286	VSS
48	VSS	94	DQS9_B_c, TDQS9_B_c	143	VSS	192	DQ30_A	238	DQS4_B_c	287	DQ31_B
49	DQ29_A	95	VSS	144	RFU	193	VSS	239	DQS4_B_t	288	VSS

Function Block Diagram

1Rank, x8 DDR5 SDRAMs



[NOTE] 1. Unless otherwise noted resistors are 15 Ω ± 5%
2. ZQ resistors are 240 Ω ± 1%.

Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Note
Operating Temperature	TOPER	0 to 85	°C	1,2

Note: Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on V_{DD} relative to Vss	VDD	-0.3 ~ 1.4	V	1
Voltage on V_{DDQ} pin relative to Vss	VDDQ	-0.3 ~ 1.4	V	1
Voltage on any pin relative to Vss	VIN, VOUT	-0.3 ~ 1.4	V	1
Storage temperature	T_{STG}	-55~+100	°C	1,2

Note:
1. Stress greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

AC & DC Operating Conditions

Recommended DC operating conditions

Parameter	Symbol	Voltage	Rating			Unit	Notes
			Min	Typ.	Max		
Host Supply Voltage	VIN_BULK	12.0	4.25	12.0	15.0	V	
PMIC Output Supply Voltage	VDD	1.1	1.067	1.1	1.166	V	1,2,3
PMIC Output Supply Voltage	VDDQ	1.1	1.067	1.1	1.166	V	1,2,3
PMIC Output Supply Voltage	VPP	1.8	1.746	1.8	1,908	V	3
AC Input Logic High	$V_{IH(AC)}$	TBD	-	-	-	mV	
AC Input Logic Low	$V_{IL(AC)}$	TBD	-	-	-	mV	
DC Input Logic High	$V_{IH(DC)}$	TBD	-	-	-	mV	
DC Input Logic Low	$V_{IL(DC)}$	TBD	-	-	-	mV	

Note: (1) VDD must be within 66mv of VDDQ
(2) AC parameters are measured with VDD and VDDQ tied together.
(3) This includes all voltage noise from DC to 2 MHz at the DRAM package ball.

IDD Specification parameters Definition - 16GB

Symbol	Condition	16GB	Unit
IDD0	One bank ACTIVATE-PRECHARGE current	TBD	mA
IDD0F	Operating Four Bank Active-Precharge Current	TBD	mA
IDD2N	Precharge Standby Current	TBD	mA
IDD2P	Precharge Power-Down Current	TBD	mA
IDD3N	Active standby current	TBD	mA
IDD3P	Active Power-Down Current	TBD	mA
IDD4R	Burst Read Current	TBD	mA
IDD4W	Burst write current	TBD	mA
IDD5B	Burst Refresh Current (1x REF)	TBD	mA
IDD6N	Self refresh current: Normal temperature range (0–85°C)	TBD	mA
IDD7	Bank interleave read current	TBD	mA
IDD8	Maximum power-down current	TBD	mA

■ Timing Parameters & Specifications

Parameter	Symbol	DDR5-4400		DDR5-4800		DDR5-5200		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Clock Timing									
Clock period average	tCK (AVG)	0.5	<0.500	0.4	<0.454	0.4	<0.416	ns	1
Command and Address Timing									
Read to Read command delay for same bank group	tCCD_L	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	nCK,ns	
Write to Write command delay for same bank groupp	tCCD_L_WR	max(32nCK, 20ns)	–	max(32nCK, 20ns)	–	max(32nCK, 20ns)	–	nCK,ns	
Write to Write command delay for same bank group, second write not RMW	tCCD_L_WR2	max(16nCK, 10ns)	–	max(16nCK, 10ns)	–	max(16nCK, 10ns)	–	nCK,ns	
Read to Write command delay for same bank group	tCCD_L_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3,5,6
Write to Read command delay for same bank group	tCCD_L_WTR	CWL + WBL/2 + Max(16nCK,10ns)						nCK,ns	4,6
Read to Read command delay for different bank group	tCCD_S	8	–	8	–	8	–	nCK	
Write to Write command delay for different bank group	tCCD_S_WR	8	–	8	–	8	–	nCK	
Read to Write command delay for different bank group	tCCD_S_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3,5,6
Write to Read command delay for different bank group	tCCD_S_WTR	CWL + WBL/2 + Max(4nCK,2.5ns)						nCK,ns	4,6
Write to Read with Auto Precharge command delay for same bank	tCCD_WTRA	CWL + WBL/2 + tWR - tRTP						nCK,ns	2,4,6

Parameter	Symbol	DDR5-4400		DDR5-4800		DDR5-5200		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Activate to Activate command delay to same bank group for 1KB page size	tRRD_L(1K)	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	nCK,ns	
Activate to Activate command delay to same bank group for 2KB page size	tRRD_L(2K)	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	nCK,ns	
Activate to Activate command delay to different bank group for 1KB page size	tRRD_S(1K)	8	–	8	–	8	–	nCK	
Activate to Activate command delay to different bank group for 2KB page size	tRRD_S(2K)	8	–	8	–	8	–	nCK	
Four activate window for 1KB page size	tFAW (1K)	Max(32nCK, 14.545ns)	–	Max(32nCK, 13.333ns)	–	Max(32nCK, 12.307ns)	–	nCK,ns	
Four activate window for 2KB page size	tFAW (2K)	Max(40nCK, 18.181ns)	–	Max(40nCK, 16.666ns)	–	Max(40nCK, 15.384ns)	–	nCK,ns	
Read to Precharge command delay	tRTP	Max(12nCK, 7.5ns)	–	Max(12nCK, 7.5ns)	–	Max(12nCK, 7.5ns)	–	nCK,ns	
Precharge to Precharge command delay	tPPD	2	–	2	–	2	–	nCK	7
Write recovery time	tWR	30	–	30	–	30	–	ns	

Notes:

1. tCK(avg)min listed for reference only, refer to the Speed Bins and Operations section which lists all valid tCK(avg) values.

2. tCCD_WTRA(min) shall always be greater than or equal to CWL + WBL/2 + tWR(min) - tRTP(min), and when using the appropriate rounding algorithms,

   nCCD_WTRA(min) shall always be greater than or equal to CWL + WBL/2 + nWR(min) - nRTP(min).

3. RBL: Read burst length associated with Read command

   RBL = 32 (36 w/ RCRC on) for fixed BL32 and BL32 in BL32 OTF mode

   RBL = 16 (18 w/ RCRC on) for fixed BL16 and BL16 in BL32 OTF mode

   RBL = 16 (18 w/ RCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode

4. WBL: Write burst length associated with Write command

   WBL = 32 (36 w/ WCRC on) for fixed BL32 and BL32 in BL32 OTF mode

   WBL = 16 (18 w/ WCRC on) for fixed BL16 and BL16 in BL32 OTF mode

   WBL = 16 (18 w/ WCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode

5. 5 - The following is considered for tRTW equation

   1tCK needs to be added due to tDQS2CK

   Read DQS offset timing can pull in the tRTW timing

   1tCK needs to be added when 1.5tCK postamble

6. CWL=CL-2

7. tPPD applies to any combination of precharge commands (PREab, PREsb, PREpb). tPPD also applies to any combination of precharge commands to a different die in a 3DS DDR5 SDRAM.

■ SERIAL PRESENCE DETECT SPECIFICATION

Byte	Function Described	Function		HEX Value
0	Number of Bytes in SPD Device	SPD Total: 1024Bytes, 3~0: Beta Level		30
1	SPD Revision for Base Configuration Parameters	Version 1.0		10
2	Key Byte / Host Bus Command Protocol Type	DDR5 SDRAM		12
3	Key Byte / Module Type	R-DIMM		01
4	First SDRAM Density and Package	Monolithic SDRAM	16Gb	04
5	First SDRAM Addressing	Row : 16	Column : 10	00
6	First SDRAM I/O Width	x8		20
7	First SDRAM Bank Groups & Banks Per Bank Group	8 bank groups/4 banks per bank group		62
8	Second SDRAM Density and Package			00
9	Second SDRAM Addressing			00
10	Secondary SDRAM I/O Width			00
11	Second SDRAM Bank Groups & Banks Per Bank Group			00
12	SDRAM BL32 & Post Package Repair	One repair element per bank	Burst length 32 supported	90
13	SDRAM Duty Cycle Adjuster & Partial Array Self Refresh	Device supports DCA for 4-phase internal clock(s)		02
14	SDRAM Fault Handling	Writeback suppression control in MR9		00
15	Reserved	must be coded as 0x00		00
16	SDRAM Nominal Voltage, VDD	Operable:1.1V	Endurant:1.1V	00
17	SDRAM Nominal Voltage, VDDQ	Operable:1.1V	Endurant:1.1V	00
18	SDRAM Nominal Voltage, VPP	Operable:1.8V	Endurant:1.8V	00
19	SDRAM Timing	Standard core timings per JESD79-5		00
20	SDRAM Minimum Cycle Time (tCKAVGmin), Least Significant Byte	416 ps		A0
21	SDRAM Minimum Cycle Time (tCKAVGmin), Most Significant Byte			01
22	SDRAM Maximum Cycle Time (tCKAVGmax), Least Significant Byte	1010 ps		F2
23	SDRAM Maximum Cycle Time (tCKAVGmax), Most Significant Byte			03
24	SDRAM CAS Latencies Supported:First Byte	CL22,26,28,30,32		7A
25	SDRAM CAS Latencies Supported:Second Byte	CL36,40,42		0D
26	SDRAM CAS Latencies Supported:Third Byte	-		00
27	SDRAM CAS Latencies Supported:Fourth Byte	-		00
28	SDRAM CAS Latencies Supported:Fifth Byte	-		00
29	Reserved	must be coded as 0x00		00
30	SDRAM Minimum CAS Latency Time (tAAmin), Least Significant Byte	16000 ps		80
31	SDRAM Minimum CAS Latency Time (tAAmin), Most Significant Byte			3E
32	SDRAM Minimum RAS to CAS Delay Time (tRCDmin), Least Significant Byte	16000 ps		80
33	SDRAM Minimum RAS to CAS Delay Time (tRCDmin), Most Significant Byte			3E
34	SDRAM Minimum Row Precharge Delay Time (tRPmin), Least Significant Byte	16000 ps		80
35	SDRAM Minimum Row Precharge Delay Time (tRPmin), Most Significant Byte			3E
36	SDRAM Minimum Active to Precharge Delay Time (tRASmin), Least Significant Nibble	32000 ps		00
37	SDRAM Minimum Active to Precharge Delay Time (tRASmin), Most Significant Byte			7D
38	SDRAM Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Nibble	48000 ps		80
39	SDRAM Minimum Active to Active/Refresh Delay Time (tRCmin), Most Significant Nibble			BB
40	SDRAM Minimum Write Recovery Time (tWRmin), Least Significant Nibble	30000 ps		30
41	SDRAM Minimum Write Recovery Time (tWRmin), Most Significant Nibble			75
42	SDRAM Minimum Refresh Recovery Delay Time (tRFC1min, tRFC1_slr min),Least Significant Byte	295 ns		27
43	SDRAM Minimum Refresh Recovery Delay Time (tRFC1min, tRFC1_slr min),Most Significant Byte			01
44	SDRAM Minimum Refresh Recovery Delay Time (tRFC2min, tRFC2_slr min),Least Significant Byte	160 ns		A0
45	SDRAM Minimum Refresh Recovery Delay Time (tRFC2min, tRFC2_slr min),Most Significant Byte			00
46	SDRAM Minimum Refresh Recovery Delay Time (tRFCsbmin, tRFCsb_slr min),Least Significant Byte	130 ns		82
47	SDRAM Minimum Refresh Recovery Delay Time (tRFCsbmin, tRFCsb_slr min),Most Significant Byte			00
48	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFC1_dlr min),Least Significant Byte	monolithic SDRAMs		00
49	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFC1_dlr min),Most Significant Byte			00
50	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFC2_dlr min),Least Significant Byte	monolithic SDRAMs		00
51	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFC2_dlr min),Most Significant Byte			00
52	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFCsb_dlr min),Least Significant Byte	monolithic SDRAMs		00
53	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFCsb_dlr min),Most Significant Byte			00
54	SDRAM Refresh Management, First Byte, First SDRAM	RAAMMT/RAAIMT/RFM Required		00
55	SDRAM Refresh Management, Second Byte, First SDRAM	RFM RAA/ARFM Level		00
56	SDRAM Refresh Management, First Byte, Second SDRAM	RAAMMT/RAAIMT/RFM Required		00
57	SDRAM Refresh Management, Second Byte, Second SDRAM	RFM RAA/ARFM Level		00
58	SDRAM Adaptive Refresh Management, First SDRAM, First Byte,Level A			00
59	SDRAM Adaptive Refresh Management, First SDRAM, Second Byte,Level A			00
60	SDRAM Adaptive Refresh Management, Second SDRAM, First Byte,Level A			00
61	SDRAM Adaptive Refresh Management, Second SDRAM, Second Byte,Level A			00
62	SDRAM Adaptive Refresh Management, First SDRAM, First Byte,Level B			00
63	SDRAM Adaptive Refresh Management, First SDRAM, Second Byte,Level B			00
64	SDRAM Adaptive Refresh Management, Second SDRAM, First Byte,Level B			00

65	SDRAM Adaptive Refresh Management, Second SDRAM, Second Byte,Level B			00
66	SDRAM Adaptive Refresh Management, First SDRAM, First Byte,Level C			00
67	SDRAM Adaptive Refresh Management, First SDRAM, Second Byte,Level C			00
68	SDRAM Adaptive Refresh Management, Second SDRAM, First Byte,Level C			00
69	SDRAM Adaptive Refresh Management, Second SDRAM, Second Byte,Level C			00
70	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group,(tRRD_Lmin),Least Significant Byte	5000	ps	88
71	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group,(tRRD_Lmin),Most Significant Byte			13
72	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group,(tRRD_Lmin),Lower Clock Limit	8	nCK	08
73	SDRAM Minimum CAS_n to CAS_n Command Delay Time, Same Bank Group,(tCCD_Lmin),Least Significant Byte	5000	ps	88
74	SDRAM Minimum CAS_n to CAS_n Command Delay Time, Same Bank Group,(tCCD_Lmin),Most Significant Byte			13
75	SDRAM Minimum CAS_n to CAS_n Command Delay Time, Same Bank Group,(tCCD_Lmin),Lower Clock Limit	8	nCK	08
76	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group (tCCD_L_WRmin),Least Significant Byte	20000	ps	20
77	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group (tCCD_L_WRmin),Most Significant Byte			4E
78	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group (tCCD_L_WRmin),Lower Clock Limit	32	nCK	20
79	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group (tCCD_L_WR2min),Least Significant Byte	10000	ps	10
80	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group (tCCD_L_WR2min),Most Significant Byte			27
81	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group (tCCD_L_WR2min),Lower Clock Limit	16	nCK	10
82	SDRAM Minimum Four Activate Window (tFAWmin),Least Significant Byte	13333	ps	15
83	SDRAM Minimum Four Activate Window (tFAWmin),Most Significant Byte			34
84	SDRAM Minimum Four Activate Window (tFAWmin),Lower Clock Limit	32	nCK	20
85	SDRAM Minimum Internal Write to Read Command Delay Time, Same Bank Group,(tWTR_Lmin),Least Significant Byte	10000	ps	10
86	SDRAM Minimum Internal Write to Read Command Delay Time, Same Bank Group,(tWTR_Lmin),Most Significant Byte			27
87	SDRAM Minimum Internal Write to Read Command Delay Time, Same Bank Group,(tWTR_Lmin),Lower Clock Limit	16	nCK	10
88	SDRAM Minimum Internal Write to Read Command Delay Time, Same Bank Group,(tWTR_Smin),Least Significant Byte	2500	ps	C4
89	SDRAM Minimum Internal Write to Read Command Delay Time, Same Bank Group,(tWTR_Smin),Most Significant Byte			09
90	SDRAM Minimum Internal Write to Read Command Delay Time, Same Bank Group,(tWTR_Smin),Lower Clock Limit	4	nCK	04
91	SDRAM Minimum Internal Read to Precharge Command Delay Time, (tRTPmin),Least Significant Byte	7500	ps	4C
92	SDRAM Minimum Internal Read to Precharge Command Delay Time, (tRTPmin),Most Significant Byte			1D
93	SDRAM Minimum Internal Read to Precharge Command Delay Time, (tRTPmin),Lower Clock Limit	12	nCK	0C
94-127	Reserved, Base Configuration Section	Must be coded as 0x00		00
128-191	Reserved for future use	Reserved for future use		00
192	SPD Revision for Module Information	Version 1.0		10
193	Hashing Sequence	No authentication?		00
194	SPD Manufacturer ID Code, First Byte	MONTAGE		86
195	SPD Manufacturer ID Code, Second Byte			32
196	SPD Device Type	M88SPD5118A5-T		80
197	SPD Device Revision Number	Ver.A5		15
198	PMIC 0 Manufacturer ID Code, First Byte	MONTAGE		86
199	PMIC 0 Manufacturer ID Code, Second Byte			32
200	PMIC 0 Device Type	M88P5010 (Low-current)		81
201	PMIC 0 Revision Number	C3		33
202	PMIC 1 Manufacturer ID Code, First Byte			00
203	PMIC 1 Manufacturer ID Code, Second Byte			00
204	PMIC 1 Device Type			00
205	PMIC 1 Revision Number			00
206	PMIC 2 Manufacturer ID Code, First Byte			00
207	PMIC 2 Manufacturer ID Code, Second Byte			00
208	PMIC 2 Device Type			00
209	PMIC 2 Revision Number			00
210	Thermal Sensor Manufacturer ID Code, First Byte	MONTAGE		86
211	Thermal Sensor Manufacturer ID Code, Second Byte			32
212	Thermal Sensor Device Type	M88TS5110		C1
213	Thermal Sensor Revision Number	A3		13
214	DRAM Specification Level			00
215	SPD Specification Level			00
216	PMIC0 Specification Level			00
217	PMIC1 Specification Level			00
218	PMIC2 Specification Level			00
219	TS Specification Level			00
220	DIMM Specification Level			00
221-229	Reserved	Reserved		00
230	(Unbuffered): Module Nominal Height	31.25mm		11
231	(Unbuffered): Module Maximum Thickness	Front,1~2mm < thickness < Back, 2~3mm		21
232	(Unbuffered): Reference Raw Card Used	Raw Card D	Revision 0	03

233	(Unbuffered): DIMM Attributes	0 to +95 °C/ 2 row DRAM	82
234	(Unbuffered): Module Organization	Symmetrical/1 Package Ranks	00
235	Memory Channel Bus Width	2 channels/32 bits,8 bits ECC	32
236-239	Reserved	must be coded as 0x00	00
240	Registering Clock Driver Manufacturer ID Code, First Byte	MONTAGE	86
241	Registering Clock Driver Manufacturer ID Code, Second Byte		32
242	Registering Clock Driver Device Type	M88DR5RCD01	80
243	Registering Clock Driver Device Revision	B2	22
244	Data Buffers Manufacturer ID Code, First Byte		00
245	Data Buffers Manufacturer ID Code, Second Byte		00
246	Data Buffers Device Type		00
247	Data Buffers Device Revision		00
248	RCD-RW08 Clock Driver Enable	BCK_t/_c - disabled, QDCK_t/_c - disable, QCCK_t/_c - disable / QBCK_t/_c - disable, QACK_t/_c - disable	2E
249	RCD-RW09 Output Address and Control Enable	QBCS[1:0]_n output - disable, QACS[1:0]_n output - enable, Q[B:A]CA13 output driver - enable, BCS_n, BCOM[2:0] & BRST_n outputs - disable, DCS1_n input buffer & QxCS1_n outputs - disable, QBCA outputs - disable, QACA outputs - enable	4E
250	RCD-RW0A QCK Driver Characteristics	RCD-RW0A QCK Driver Characteristics - only QACK_t/QACK_c - enabled (20 ohm)	00
251	RCD-RW0B	must be coded as 0x00	00
252	RCD-RW0C QxCA and QxCS_n Driver Characteristics	RCD-RW0C QxCA and QxCS_n Driver Characteristics both 20 ohm	00
253	RCD-RW0D Data Buffer Interface Driver Characteristics		00
254	RCD-RW0E QCK, QCA, and QCS Output Slew Rate	RCD-RW0E QCK - mod, QCA - slow and QCS – slow , Output Slew Rate	28
255~447	(Unbuffered):Module Type Specific Information	Reserved	00
448-509	Reserved for future use	-	00
510	CRC for Byte 0~509,Least Significant Byte	CRC	77
511	CRC for Byte 0~509,Most Significant Byte	CRC	DB
512	Module Manufacturer ID Code, First Byte		04
513	Module Manufacturer ID Code, Second Byte		CB
514	Module Manufacturing Location	*Note: 1 (Decimal)	-
515	Module Manufacturing Date	*Note: 2 (Decimal)	-
516	Module Manufacturing Date	*Note: 3 (Decimal)	-
517	Module Serial Number	*Note: 4 (Decimal)	-
518			-
519			-
520			-
550	Module Part Number	*Note: 5	-
551	Module Revision Code		00
552	DRAM Manufacturer ID Code, First Byte	*Note: 7	-
553	*DRAM* Manufacturer ID Code, Second Byte		-
554	DRAM Stepping	Undefined/Stepping information not provided	FF
555-639	Manufacturer's Specific Data	*Note: 8	-
640	Intel Extreme Memory Profile Identification String		00
641	Intel Extreme Memory Profile Identification String		00
642	Intel Extreme Memory Profile Version		00
643	Intel Extreme Memory Profile Organization		00
644	Intel Extreme Memory Profile Configuration		00
645	PMIC Vendor ID		00
646	PMIC Vendor ID		00
647	Number of PMICs		00
648	PMIC Capabilities		00
649-653	RSVD		00
654~701	Profile 1/2/3 String Name		00
702~895	Profile 1/2/3 Parameter		00
896-1023	User Settings		00

Note :
1. Byte 194-201 -- By SPD_Hub & PMIC Vendor & Revision
1.1 Byte 194-197 – RENESAS[(0x80), (0xB3), (0x80), (0x21)] ; MONTAGE[(0x86), (0x32), (0x80), (0x15)]
1.2 Byte 198-201 – RENESAS[(0x80), (0xB3), (0x82), (0x11)] ; MONTAGE[(0x86), (0x32), (0x81), (0x33)]

2. Byte 514 -- Manufacturing location by manufacturing location
3. Byte 515 -- Module manufacturing date by year (YY). (Decimal)
4. Byte 516 -- Module manufacturing date by week (WW). (Decimal)
5. Bytes 517-520 -- Module Serial Number. (Decimal)
6. Bytes 521-550 -- Module Part Number. (ASCII format, unused digits are coded as ASCII blanks (0x20).
7. Bytes 552-553 -- DRAM Manufacturer ID Code by JEDEC definition. SAMSUNG :[(0x80) ,(0xCE)]
8. Bytes 555~639 -- These bytes are undefined and can be used own purpose.