

Advantech

AQD-SD3L8GN16-SGH

Datasheet

Rev. 1.0

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Description

DDR3 1.35V SO-DIMM is high-speed, low power memory module that use 512Mx8bits DDR3 SDRAM in FBGA package and a 2048 bits serial EEPROM on a 204-pin printed circuit board. DDR3 1.35V SO-DIMM is a Dual In-Line Memory Module and is intended for mounting into 204-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

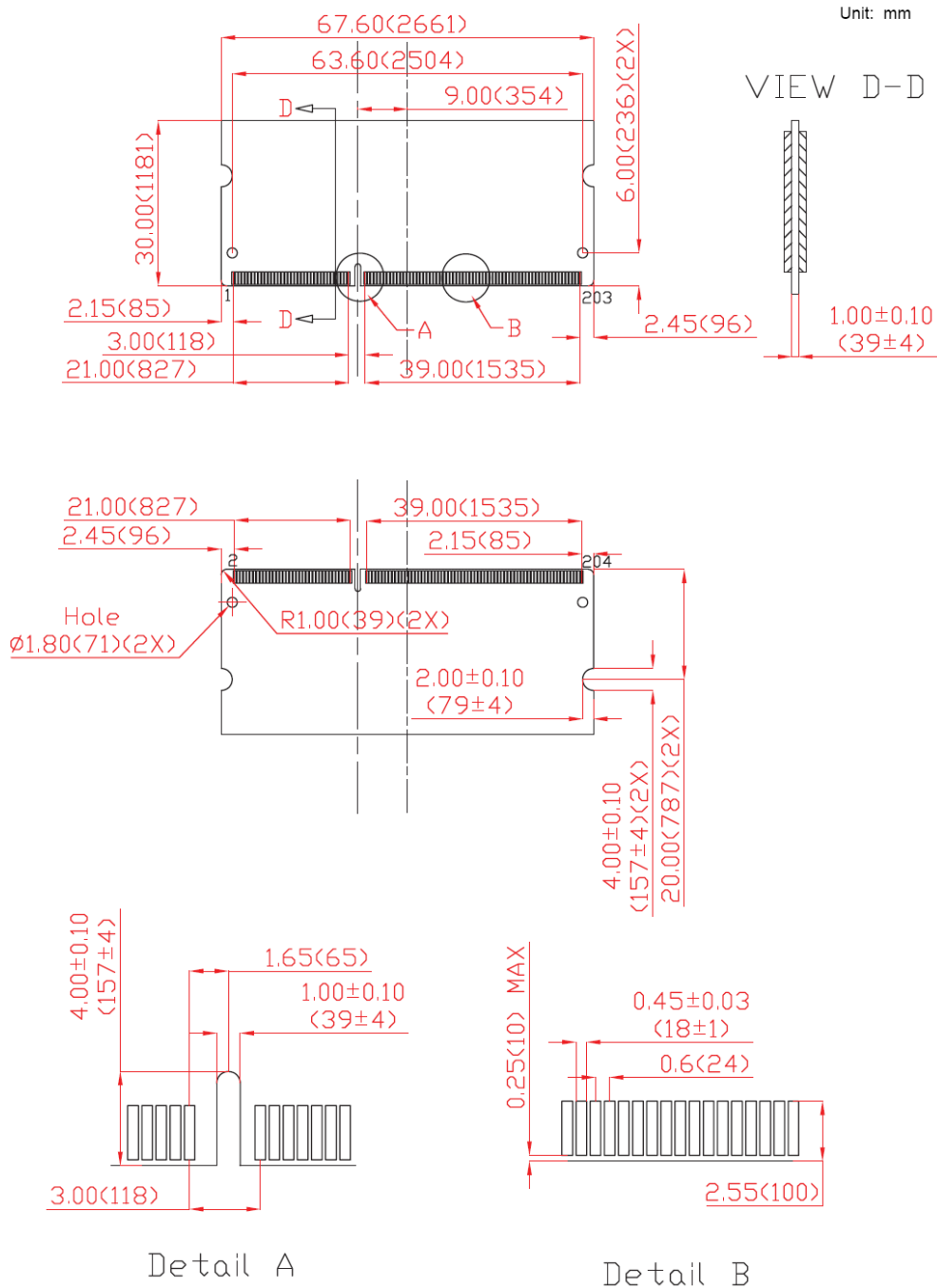
Features

- RoHS compliant products.
- JEDEC standard 1.35V(1.283V~1.45V) Power supply
- VDDQ=1.35V(1.28V~1.45V)
- Clock Freq: 800MHZ for 1600Mb/s/Pin.
- Programmable CAS Latency: 6, 7, 8, 9, 10, 11
- Programmable Additive Latency (Posted /CAS):
0,CL-2 or CL-1 clock
- Programmable /CAS Write Latency (CWL)
= 8(DDR3-1600)
- 8 bit pre-fetch
- Burst Length: 4, 8
- Bi-directional Differential Data-Strobe
- Internal calibration through ZQ pin
- On Die Termination with ODT pin
- Serial presence detect with EEPROM
- Asynchronous reset
- PCB: 30μ inch gold finger
- Anti-Sulfuration (Anti-FOS test: ASTM-B809-95)

Pin Identification

| Symbol | Function |
|---------------------|--|
| A0~A15, BA0~BA2 | Address/Bank input |
| DQ0~DQ63 | Bi-direction data bus. |
| DQS0~DQS7 | Data strobes |
| /DQS0~/DQS7 | Differential Data strobes |
| CK0, /CK0,CK1, /CK1 | Clock Input. (Differential pair) |
| CKE0, CKE1 | Clock Enable Input. |
| ODT0, ODT1 | On-die termination control line |
| /S0, /S1 | DIMM rank select lines. |
| /RAS | Row address strobe |
| /CAS | Column address strobe |
| /WE | Write Enable |
| DM0~DM7 | Data masks/high data strobes |
| VDD | Core power supply |
| VDDQ | I/O driver power supply |
| V _{REFDQ} | I/O reference supply |
| V _{REFCA} | Command/address reference supply |
| V _{DDSPD} | SPD EEPROM power supply |
| SA0~SA2 | I2C serial bus address select for EEPROM |
| SCL | I2C serial bus clock for EEPROM |
| SDA | I2C serial bus data for EEPROM |
| VSS | Ground |
| /RESET | Set DRAMs Known State |
| VTT | SDRAM I/O termination supply |
| NC | No Connection |

Dimensions (Unit: millimeter)



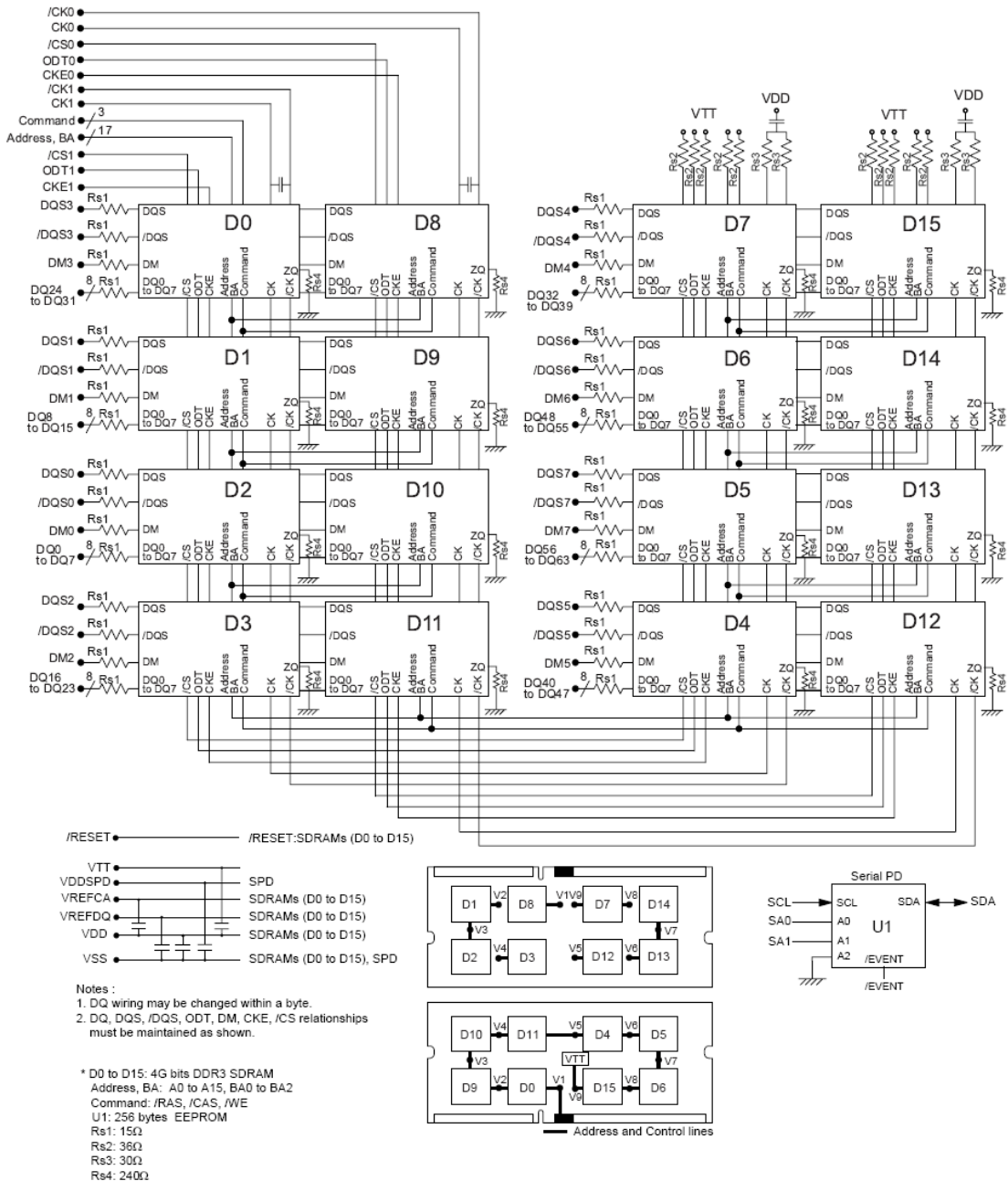
(All dimensions are in millimeters with $\pm 0.15\text{mm}$ tolerance unless specified otherwise.)

Pin Assignments

| Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name |
|---------|----------|---------|----------|---------|----------|---------|----------|---------|----------|---------|----------|---------|----------|---------|----------|
| 1 | VREFDQ | 53 | DQ19 | 105 | VDD | 157 | DQ42 | 2 | VSS | 54 | VSS | 106 | VDD | 158 | DQ46 |
| 3 | VSS | 55 | VSS | 107 | A10(AP) | 159 | DQ43 | 4 | DQ4 | 56 | DQ28 | 108 | BA1 | 160 | DQ47 |
| 5 | DQ0 | 57 | DQ24 | 109 | BA0 | 161 | VSS | 6 | DQ5 | 58 | DQ29 | 110 | /RAS | 162 | VSS |
| 7 | DQ1 | 59 | DQ25 | 111 | VDD | 163 | DQ48 | 8 | VSS | 60 | VSS | 112 | VDD | 164 | DQ52 |
| 9 | VSS | 61 | VSS | 113 | /WE | 165 | DQ49 | 10 | /DQS0 | 62 | /DQS3 | 114 | /CS0 | 166 | DQ53 |
| 11 | DM0 | 63 | DM3 | 115 | /CAS | 167 | VSS | 12 | DQS0 | 64 | DQS3 | 116 | ODT0 | 168 | VSS |
| 13 | VSS | 65 | VSS | 117 | VDD | 169 | /DQS6 | 14 | VSS | 66 | VSS | 118 | VDD | 170 | DM6 |
| 15 | DQ2 | 67 | DQ26 | 119 | A13 | 171 | DQS6 | 16 | DQ6 | 68 | DQ30 | 120 | ODT1 | 172 | VSS |
| 17 | DQ3 | 69 | DQ27 | 121 | /CS1 | 173 | VSS | 18 | DQ7 | 70 | DQ31 | 122 | NC | 174 | DQ54 |
| 19 | VSS | 71 | VSS | 123 | VDD | 175 | DQ50 | 20 | VSS | 72 | VSS | 124 | VDD | 176 | DQ55 |
| 21 | DQ8 | 73 | CKE0 | 125 | NC | 177 | DQ51 | 22 | DQ12 | 74 | CKE1 | 126 | VREFCA | 178 | VSS |
| 23 | DQ9 | 75 | VDD | 127 | VSS | 179 | VSS | 24 | DQ13 | 76 | VDD | 128 | VSS | 180 | DQ60 |
| 25 | VSS | 77 | NC | 129 | DQ32 | 181 | DQ56 | 26 | VSS | 78 | A15(NC) | 130 | DQ36 | 182 | DQ61 |
| 27 | /DQS1 | 79 | BA2 | 131 | DQ33 | 183 | DQ57 | 28 | DM1 | 80 | A14(NC) | 132 | DQ37 | 184 | VSS |
| 29 | DQS1 | 81 | VDD | 133 | VSS | 185 | VSS | 30 | /RESET | 82 | VDD | 134 | VSS | 186 | /DQS7 |
| 31 | VSS | 83 | A12(BC) | 135 | /DQS4 | 187 | DM7 | 32 | VSS | 84 | A11 | 136 | DM4 | 188 | DQS7 |
| 33 | DQ10 | 85 | A9 | 137 | DQS4 | 189 | VSS | 34 | DQ14 | 86 | A7 | 138 | VSS | 190 | VSS |
| 35 | DQ11 | 87 | VDD | 139 | VSS | 191 | DQ58 | 36 | DQ15 | 88 | VDD | 140 | DQ38 | 192 | DQ62 |
| 37 | VSS | 89 | A8 | 141 | DQ34 | 193 | DQ59 | 38 | VSS | 90 | A6 | 142 | DQ39 | 194 | DQ63 |
| 39 | DQ16 | 91 | A5 | 143 | DQ35 | 195 | VSS | 40 | DQ20 | 92 | A4 | 144 | VSS | 196 | VSS |
| 41 | DQ17 | 93 | VDD | 145 | VSS | 197 | SA0 | 42 | DQ21 | 94 | VDD | 146 | DQ44 | 198 | /EVENT |
| 43 | VSS | 95 | A3 | 147 | DQ40 | 199 | VDDSPD | 44 | VSS | 96 | A2 | 148 | DQ45 | 200 | SDA |
| 45 | /DQS2 | 97 | A1 | 149 | DQ41 | 201 | SA1 | 46 | DM2 | 98 | A0 | 150 | VSS | 202 | SCL |
| 47 | DQS2 | 99 | VDD | 151 | VSS | 203 | VTT | 48 | VSS | 100 | VDD | 152 | /DQS5 | 204 | VTT |
| 49 | VSS | 101 | CK0 | 153 | DM5 | | | 50 | DQ22 | 102 | CK1 | 154 | DQS5 | | |
| 51 | DQ18 | 103 | /CK0 | 155 | VSS | | | 52 | DQ23 | 104 | /CK1 | 156 | VSS | | |

Note: 1. /CS1,ODT1,CKE1 : Used for dual-rank SO-DIMMs; NC on single-rank SO-DIMMs.
2. CK1 and /CK1 : Used for dual-rank SO-DIMMs; not used on single-rank SO-DIMMs but terminated.

Block Diagram 8GB, 1Gx64 Module(2 Rank x8)



This technical information is based on industry standard data and tests believed to be reliable. However, Advantech makes no warranties, either expressed or implied, as to its accuracy and assume no liability in connection with the use of this product. Advantech reserves the right to make changes in specifications at any time without prior notice.

Operating Temperature Condition

| Parameter | Symbol | Rating | Unit | Note |
|-----------------------|--------|-----------|------|------|
| Operating Temperature | TOPER | -20 to 85 | °C | 1,2 |

Note: 1. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
 2. At 0 - 85C, operation temperature range are the temperature which all DRAM specification will be supported.

Absolute Maximum DC Ratings

| Parameter | Symbol | Value | Unit | Note |
|-------------------------------------|-----------|--------------|------|------|
| Voltage on VDD relative to Vss | VDD | -0.4 ~ 1.975 | V | 1 |
| Voltage on VDDQ pin relative to Vss | VDDQ | -0.4 ~ 1.975 | V | 1 |
| Voltage on any pin relative to Vss | VIN, VOUT | -0.4 ~ 1.975 | V | 1 |
| Storage temperature | TSTG | -55~+100 | °C | 1,2 |

Note: 1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
 2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

AC & DC Operating Conditions

Recommended DC operating conditions

| Parameter | Symbol | Voltage | Rating | | | Unit | Notes |
|---------------------------------|-------------------------|---------|------------|-----------|------------|------|-------|
| | | | Min | Typ. | Max | | |
| Supply voltage | VDD | 1.35V | 1.283 | 1.35 | 1.45 | V | 1, 2 |
| | | 1.5V | 1.425 | 1.5 | 1.575 | | |
| Supply voltage for Output | VDDQ | 1.35V | 1.283 | 1.35 | 1.45 | V | 1, 2 |
| | | 1.5V | 1.425 | 1.5 | 1.575 | | |
| I/O Reference Voltage (DQ) | VREF _{DQ} (DC) | 1.35V | 0.49*VDDQ | 0.50*VDDQ | 0.51*VDDQ | V | 3 |
| I/O Reference Voltage (CMD/ADD) | VREF _{CA} (DC) | 1.5V | 0.49*VDDQ | 0.50*VDDQ | 0.51*VDDQ | V | 3 |
| AC Input Logic High | VIH(AC) | 1.35V | VREF+0.160 | - | - | V | |
| | | 1.5V | VREF+0.175 | - | - | | |
| AC Input Logic Low | VIL(AC) | 1.35V | - | - | VREF-0.160 | V | |
| | | 1.5V | - | - | VREF-0.175 | | |
| DC Input Logic High | VIH(DC) | 1.35V | VREF+0.09 | - | VDD | V | |
| | | 1.5V | VREF+0.1 | - | VDD | | |
| DC Input Logic Low | VIL(DC) | 1.35V | VSS | - | VREF-0.09 | V | |
| | | 1.5V | VSS | - | VREF-0.1 | | |

Note: 1. Under all conditions VDDQ must be less than or equal to VDD.
 2. VDDQ tracks with VDD, AC parameters are measured with VDD and VDDQ tied together.
 3. Peak to peak AC noise on VREF may not allow deviate from VREF(DC) by more than +/-1% VDD.

IDD Specification parameters Definition(IDD values are for full operating range of Voltage and Temperature)
8GB, 1Gx64 Module(2 Rank x8)

| Parameter | Symbol | DDR3 1600 | Unit |
|---|---------|-----------|------|
| Operating One bank Active-Precharge current; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /CS is HIGH between valid commands;Address bus inputs are SWITCHING; Data bus inputs are SWITCHING | IDD0 | 472 | mA |
| Operating One bank Active-read-Precharge current; IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W | IDD1 | 528 | mA |
| Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | IDD2P-0 | 128 | mA |
| | IDD2P-1 | 160 | mA |
| Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | IDD2Q | 272 | mA |
| Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | IDD2N | 272 | mA |
| Active power - down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | IDD3P | 288 | mA |
| Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | IDD3N | 416 | mA |
| Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W | IDD4R | 888 | mA |
| Operating burst write current; All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING IDD4R | IDD4W | 928 | mA |
| Burst refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | IDD5B | 1808 | mA |
| Self refresh current; CK and /CK at 0V; CKE = 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING | IDD6 | 192 | mA |
| Self refresh temperature current (SRT-enabled): MAX TC = 95°C | IDD6ET | 256 | mA |
| Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), Trc = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS is HIGH between valid commands;Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; | IDD7 | 1288 | mA |

Note: 1. Module IDD was calculated on the specific brand DRAM(4xnm) component IDD and can be differently measured according to DQ loading capacitor.

Timing Parameters & Specifications

| Speed | | DDR3 1600 | | Unit |
|---|----------|----------------------|-------|------|
| Parameter | Symbol | Min | Max | |
| Average Clock Period | tCK | 1.25 | <1.5 | ns |
| CK high-level width | tCH | 0.47 | 0.53 | tCK |
| CK low-level width | tCL | 0.47 | 0.53 | tCK |
| DQS, /DQS to DQ skew, per group, per access | tDQSQ | - | 100 | ps |
| DQ output hold time from DQS, /DQS | tQH | 0.38 | - | tCK |
| DQ low-impedance time from CK, /CK | tLZ(DQ) | -450 | 225 | ps |
| DQ high-impedance time from CK, /CK | tHZ(DQ) | - | 225 | ps |
| Data setup time to DQS, /DQS reference to Vih(ac)Vil(ac) levels | tDS | 10 | - | ps |
| Data hold time to DQS, /DQS reference to Vih(ac)Vil(ac) levels | tDH | 45 | - | ps |
| DQ and DM input pulse width for each input | tDIPW | 360 | - | ps |
| DQS, /DQS Read preamble | tRPRE | 0.9 | - | tCK |
| DQS, /DQS differential Read postamble | tRPST | 0.3 | - | tCK |
| DQS, /DQS Write preamble | tWPRE | 0.9 | - | tCK |
| DQS, /DQS Write postamble | tWPST | 0.3 | - | tCK |
| DQS, /DQS low-impedance time | tLZ(DQS) | -450 | 225 | ps |
| DQS, /DQS high-impedance time | tHZ(DQS) | - | 225 | ps |
| DQS, /DQS differential input low pulse width | tDQSL | 0.45 | 0.55 | tCK |
| DQS, /DQS differential input high pulse width | tDQSH | 0.45 | 0.55 | tCK |
| DQS, /DQS rising edge to CK, /CK rising edge | tDQSS | -0.27 | +0.27 | tCK |
| DQS, /DQS falling edge setup time to CK, /CK rising edge | tDSS | 0.18 | - | tCK |
| DQS, /DQS falling edge hold time to CK, /CK rising edge | tDSH | 0.18 | - | tCK |
| Delay from start of Internal write transaction to Internal read command | tWTR | Max (4tck, 7.5ns) | - | |
| Write recovery time | tWR | 15 | - | ns |
| Mode register set command cycle time | tMRD | 4 | - | tCK |
| /CAS to /CAS command delay | tCCD | 4 | - | nCK |
| Auto precharge write recovery + precharge time | tDAL | tWR+tRP/tck | | nCK |
| Active to active command period for 1KB page size | tRRD | Max (4tck, 6ns) | - | ns |

| Speed | | DDR3 1600 | | Unit |
|---|----------|--------------------------|-----|------|
| Parameter | Symbol | Min | Max | |
| Active to active command period for 2KB page size | tRRD | Max (4tck, 7.5ns) | - | |
| Four Activate Window for 1KB page size | tFAW | 30 | - | ns |
| Four Activate Window for 2KB page size products | tFAW | 40 | - | ns |
| Power-up and RESET calibration time | tZQinitl | 512 | - | tCK |
| Normal operation Full calibration time | tZQoper | 256 | - | tCK |
| Normal operation short calibration time | tZQcs | 64 | - | tCK |
| Exit self refresh to commands not requiring a locked DLL | tXS | Max (5tCK, tRFC+10ns) | - | |
| Exit self refresh to commands requiring a locked DLL | tXSDLL | tDLL(min) | - | tCK |
| Internal read to precharge command delay | tRTP | Max (4tck, 7.5ns) | - | |
| Minimum CKE low width for Self refresh entry to exit timing | tCKESR | tCK(min)+1tCK | - | |
| Exit power down with DLL to any valid command: Exit Precharge Power Down with DLL | tXP | Max (3tCK, 6ns) | - | |
| CKE minimum pulse width (high and low pulse width) | tCKE | Max (3tCK, 5ns) | | |
| Asynchronous RTT turn-on delay (Power-Down mode) | tAONPD | 2 | 8.5 | ns |
| Asynchronous RTT turn-off delay (Power-Down mode) | tAOFPD | 2 | 8.5 | ns |
| ODT turn-on | tAON | -225 | 225 | ps |
| ODT turn-off | tAOF | 0.3 | 0.7 | tCK |

SERIAL PRESENCE DETECT SPECIFICATION

8192MB(1024Mx64 Bit) Serial Presence Detect for DDR3 SODIMM PC-12800 CL=11 (1.35V)

| BYTE | FUNCTION DESCRIBED | FUNCTION SUPPORTED | HEX VALUE |
|------|--|------------------------|-----------|
| 0 | Number of serial PD bytes written/SPD device size/CRC coverage | CRC 0-116/256/176 | 92 |
| 1 | SPD revision | Revision 1.3 | 13 |
| 2 | Key byte/DRAM device type | DDR3 SDRAM | 0B |
| 3 | Key byte/module type | SODIMM | 03 |
| 4 | SDRAM density and banks | 4G bits, 8 banks | 04 |
| 5 | SDRAM addressing | 16 rows, 10 columns | 21 |
| 6 | Module Nominal Voltage,VDD | Standard = 1.35V | 02 |
| 7 | Module organization | 2ranks / x8 bits | 09 |
| 8 | Module memory bus width | 64 bits | 03 |
| 9 | Fine timebase (FTB) dividend/divisor | 2018/5/2 | 52 |
| 10 | Medium timebase (MTB) dividend | 1 | 01 |
| 11 | Medium timebase (MTB) divisor | 8 | 08 |
| 12 | SDRAM minimum cycle time (tCK (min.)) | 1.25ns | 0A |
| 13 | Reserved | — | 00 |
| 14 | SDRAM /CAS latencies supported, LSB | CL=6,7,8,9,10,11 | FC |
| 15 | SDRAM /CAS latencies supported, MSB | Not support over CL=12 | 00 |
| 16 | SDRAM minimum /CAS latencies time (tAA (min.)) | 13.125ns | 69 |
| 17 | SDRAM write recovery time (tWR) | 15ns | 78 |
| 18 | SDRAM minimum /RAS to /CAS delay (tRCD) | 13.125ns | 69 |
| 19 | SDRAM minimum row active to row active delay (tRRD) | 6ns | 30 |
| 20 | SDRAM minimum row precharge time (tRP) | 13.125ns | 69 |
| 21 | SDRAM upper nibbles for tRAS and tRC | Refer to Byte22,23 | 11 |
| 22 | SDRAM minimum active to precharge time (tRAS), LSB | 35ns | 18 |
| 23 | SDRAM minimum active to active /auto- refresh time (tRC), LSB | 48.125ns | 81 |
| 24 | SDRAM minimum refresh recovery time delay (tRFC), LSB | 260ns | 20 |
| 25 | SDRAM minimum refresh recovery time delay (tRFC), MSB | 260ns | 08 |
| 26 | SDRAM minimum internal write to read command delay (tWTR) | 7.5ns | 3C |
| 27 | SDRAM minimum internal read to precharge command delay (tRTP) | 7.5ns | 3C |
| 28 | Upper nibble for tFAW | Refer to Byte29 | 00 |
| 29 | Minimum four activate window delay time (tFAW (min.)) | 30ns | F0 |

| | | | |
|--------|---|---------------------------------------|----|
| 30 | SDRAM output drivers supported | DLL-Off Mode Support/RZQ/6,7 | 83 |
| 31 | SDRAM refresh options | PASR / ASR / Normal Temp | 01 |
| 32 | Module Thermal SENSOR | not incorporated | 00 |
| 33 | SDRAM Device Type | Standard | 00 |
| 34 | Fine Offset for SDRAM Minimum Cycle Time (tCKmin) | — | 00 |
| 35 | Fine Offset for Minimum CAS Latency Time (tAAmin) | — | 00 |
| 36 | Fine Offset for Minimum RAS# to CAS# Delay Time (tRCDmin) | — | 00 |
| 37 | Fine Offset for Minimum Row Precharge Delay Time (tRPmin) | — | 00 |
| 38 | Fine Offset for Minimum Active to Active/Refresh Delay Time(tRCmin) | — | 00 |
| 39 | Reserved | — | 00 |
| 40 | Reserved | — | 00 |
| 41 | SDRAM Maximum Activate Count (MAC) Value | — | 88 |
| 42-59 | Reserved | — | 00 |
| 60 | Module nominal height | $29 < \text{height} \leq 30\text{mm}$ | 0F |
| 61 | Module maximum thickness | $\text{thickness} \leq 4 \text{ mm}$ | 11 |
| 62 | Reference raw card used | Raw Card F | 05 |
| 63 | Address mapping from edge connector to DRAM | 0 = standard | 00 |
| 64-116 | Module specific section | — | 00 |
| 117 | Module ID: manufacturer's JEDEC ID code, LSB | Advantech | 8A |
| 118 | Module ID: manufacturer's JEDEC ID code, MSB | Advantech | C8 |
| 119 | Module ID: manufacturing location | | 00 |
| 120 | Module ID: manufacturing date | Year code (BCD) | 00 |
| 121 | Module ID: manufacturing date | Week code (BCD) | 00 |
| 122 | Module ID: module serial number | | 00 |
| 123 | Module ID: module serial number | | 00 |
| 124 | Module ID: module serial number | | 00 |
| 125 | Module ID: module serial number | | 00 |
| 126 | Cyclical redundancy code (CRC) | B4 | B4 |
| 127 | Cyclical redundancy code (CRC) | B2 | B2 |
| 128 | Module part number | A | 41 |
| 129 | Module part number | Q | 51 |
| 130 | Module part number | D | 44 |

| | | | |
|---------|---|---|----|
| 131 | Module part number | - | 2D |
| 132 | Module part number | S | 53 |
| 133 | Module part number | D | 44 |
| 134 | Module part number | 3 | 33 |
| 135 | Module part number | L | 4C |
| 136 | Module part number | 8 | 38 |
| 137 | Module part number | G | 47 |
| 138 | Module part number | N | 4E |
| 139 | Module part number | 1 | 31 |
| 140 | Module part number | 6 | 36 |
| 141 | Module part number | - | 2D |
| 142 | Module part number | S | 53 |
| 143 | Module part number | G | 47 |
| 144 | Module part number | H | 48 |
| 145 | Module part number | | 20 |
| 146 | Module revision code | | 00 |
| 147 | Module revision code | | 00 |
| 148 | SDRAM manufacturer's JEDEC ID code, LSB | | 00 |
| 149 | SDRAM manufacturer's JEDEC ID code, MSB | | 00 |
| 150-175 | Manufacturer's specific data | | 00 |
| 176-255 | Open for customer use | | 00 |