Advantech

AQD-SD5V16GE48-SB
Datasheet

Rev. 1.0

2022-05-23

Description

AQD-SD5V16GE48-SB is DDR5-4800(CL40)-39-39 SDRAM memory module. The SPD is programmed to JEDEC standard latency 4800Mbps timing of 40-39-39 at 1.1V. The module is composed of 16Gb CMOS DDR5 SDRAMs in FBGA package and one 8Kbit SPD Hub in 8pin TDFN package on a 262pin glass–epoxy printed circuit board.

The module is a Dual In-line Memory Module and intended for mounting onto 262 pins edge connector sockets. Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

- RoHS compliant products.
- JEDEC standard 1.1V(1.067V~1.166V) Power supply
- VDDQ= 1.1V(1.067V~1.166V)
- VPP = 1.8V(+0.108V / -0.054V)
- Data transfer rates: PC5-4800
- Programmable CAS Latency:22,26,28,30,32,36,40,42
- 16 bit pre-fetch
- Burst Length (BL) switch on-the-fly BL16 or BC8
- Bi-directional Differential Data-Strobe
- On Die Termination, Nominal, Park
- Serial presence detect hub (SPD Hub) with Integrated Temperature sensor
- Asynchronous reset
- PCB edge connector treated with 30u” Gold-Plating

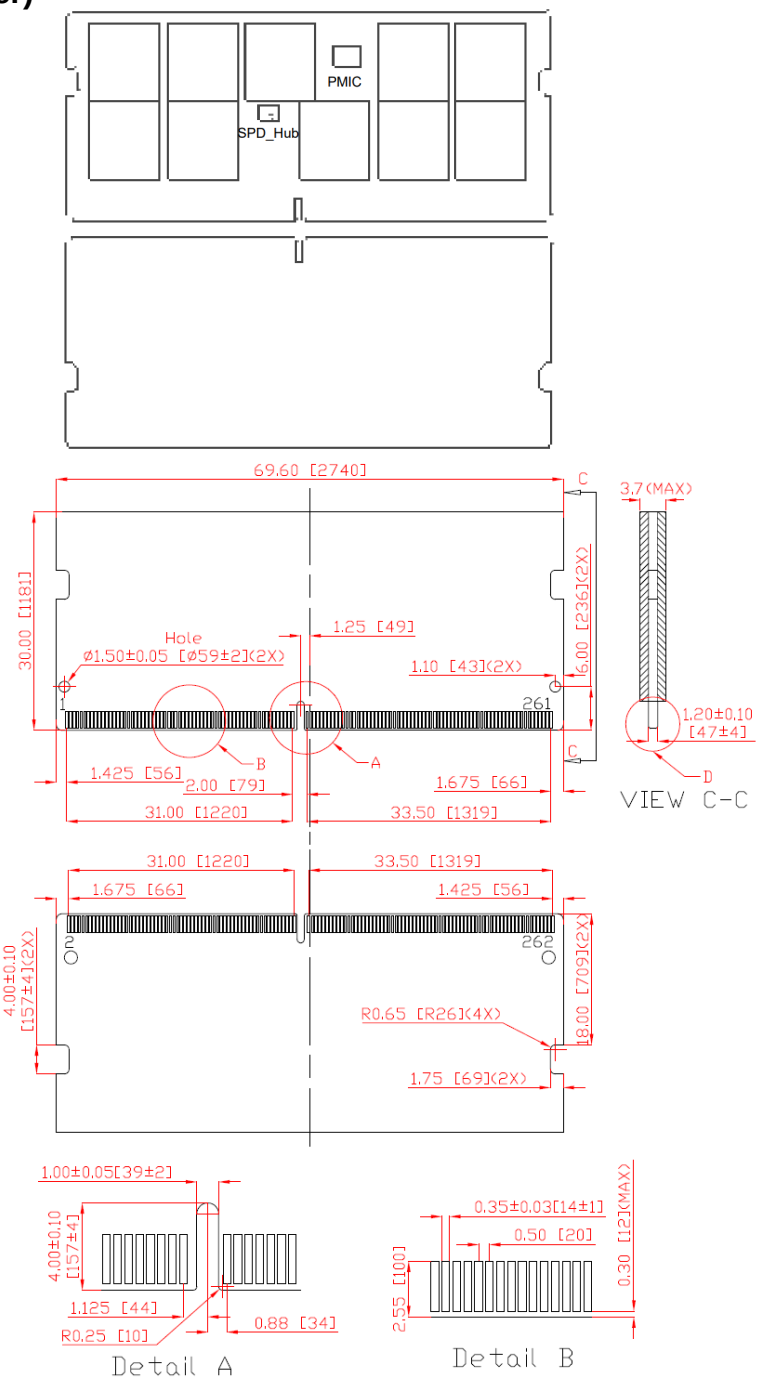
Pin Descriptions

Pin Name	Description	Pin Name	Description
CA0_A - CA12_A CA0_B - CA12_B	SDRAM Command/Address bus	HSCL	Side Band bus clock
CS0_A_n - CS1_A_n CS0_B_n - CS1_B_n	SDRAM Chip Select	HSDA	Side Band bus data
DQ0_A - DQ31_A DQ0_B - DQ31_B	DIMM memory data bus	HSA	Side Band bus address
CB0_A - CB3_A CB0_B - CB3_B	DIMM ECC check bits	ALERT_n	SDRAM ALERT_n
DQS0_A_t - DQS4_A_t DQS0_B_t - DQS4_B_t	SDRAM data strobes (positive line of differential pair)	RESET_n	Set DRAMs to a Known State
DQS0_A_c - DQS4_A_c DQS0_B_c - DQS4_B_c	SDRAM data strobes (negative line of differential pair)	VIN_BULK	5 V power input supply
DM0_A_n - DM3_A_n DM0_B_n - DM3_B_n	SDRAM data masks	VSS	Power supply return (ground)
CK0_A_t, CK1_A_t CK0_B_t, CK1_B_t	SDRAM clocks (positive line of differential pair)	PWR_GOOD	Power good indicator
CK0_A_c, CK1_A_c CK0_B_c, CK1_B_c	SDRAM clocks (negative line of differential pair)	PWR_EN	PMIC Enable
		RFU	Reserved for future use

Notes:

DDR5 SO-DIMM has 2 channels (channel-A and channel-B) of signal bus.
The signals with suffix: _A (e.g. DQ0_A) are for channel-A, and the signals with suffix: _B (e.g. DQ0_B) are for channel-B

Dimensions (Unit: millimeter)



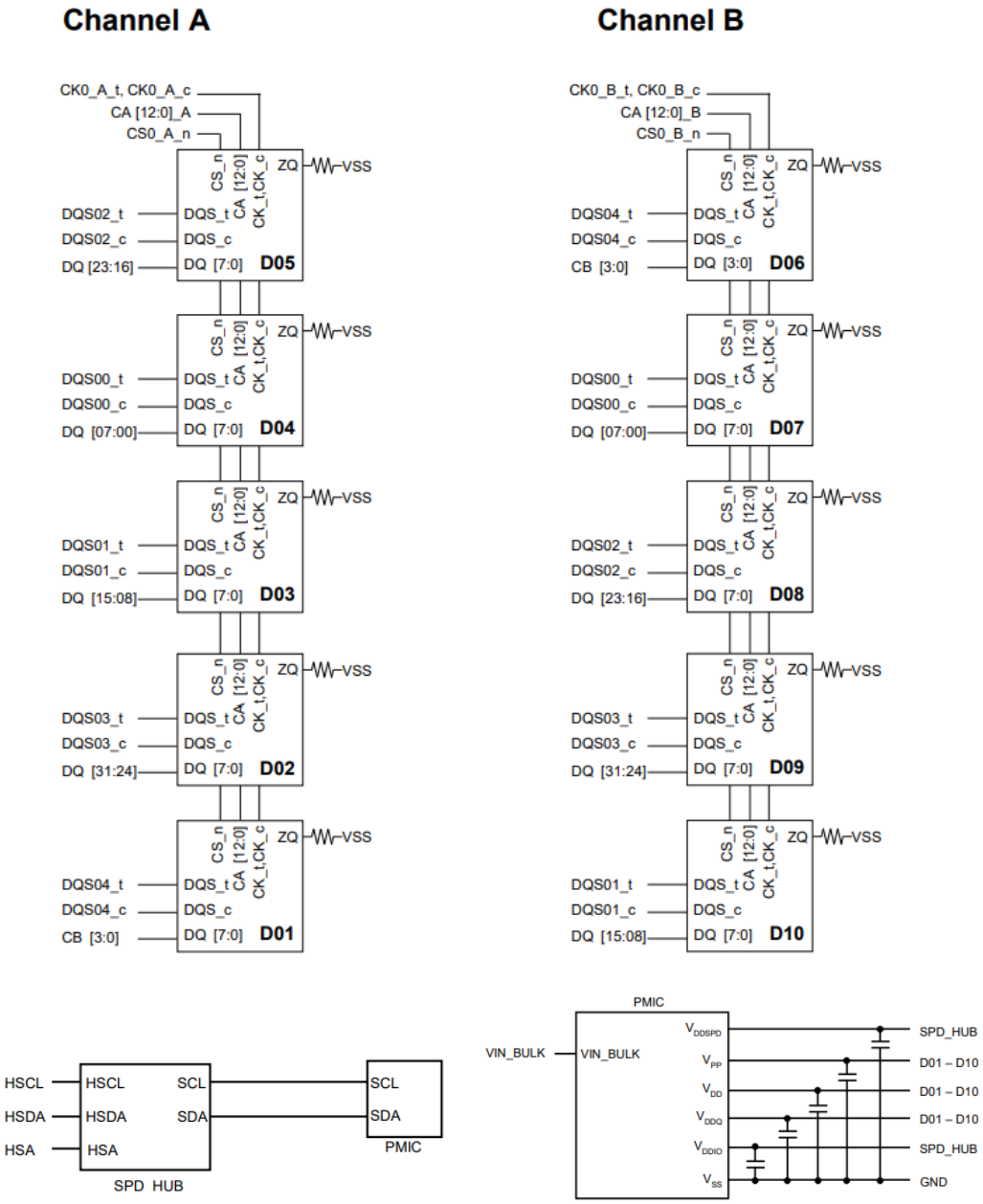
Note:1. Tolerances on all dimensions +/-0.15mm unless otherwise specified.

Pin Assignments

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VIN_BULK	89	VSS	175	CB3_B	2	HSA	90	VSS	176	CB2_B
3	VIN_BULK	91	DQ30_A	177	VSS	4	HSCL	92	DQ31_A	178	VSS
5	RFU	93	VSS	179	DQ0_B	6	HSDA	94	VSS	180	DQ1_B
7	PWR_GOOD	95	CB0_A	181	VSS	8	PWR_EN	96	CB1_A	182	VSS
9	VSS	97	VSS	183	DQ2_B	10	VSS	98	VSS	184	DQ3_B
11	DQ0_A	99	CB2_A	185	VSS	12	DQ1_A	100	DQS4_A_c	186	VSS
13	VSS	101	VSS	187	DM0_B_n	14	VSS	102	DQS4_A_t	188	DQS0_B_c
15	DQ2_A	103	CB3_A	189	VSS	16	DQ3_A	104	VSS	190	DQS0_B_t
17	VSS	105	VSS	191	DQ4_B	18	VSS	106	CS0_A_n	192	VSS
19	DM0_A_n	107	CA0_A	193	VSS	20	DQS0_A_c	108	ALERT_n	194	DQ5_B
21	VSS	109	CA1_A	195	DQ6_B	22	DQS0_A_t	110	CS1_A_n	196	VSS
23	DQ4_A	111	VSS	197	VSS	24	VSS	112	VSS	198	DQ7_B
25	VSS	113	CA2_A	199	DQ8_B	26	DQ5_A	114	CA3_A	200	VSS
27	DQ6_A	115	CA4_A	201	VSS	28	VSS	116	CA5_A	202	DQ9_B
29	VSS	117	VSS	203	DQ10_B	30	DQ7_A	118	VSS	204	VSS
31	DQ8_A	119	CA6_A	205	VSS	32	VSS	120	CA7_A	206	DQ11_B
33	VSS	121	CA8_A	207	DQS1_B_c	34	DQ09_A	122	CA9_A	208	VSS
35	DQ10_A	123	VSS	209	DQS1_B_t	36	VSS	124	VSS	210	DM1_B_n
37	VSS	125	CA10_A	211	VSS	38	DQ11_A	126	CA11_A	212	VSS
39	DQS1_A_c	KEY		213	DQ12_B	40	VSS	KEY		214	DQ13_B
41	DQS1_A_t	127	CA12_A	215	VSS	42	DM1_A_n	128	RFU	216	VSS
43	VSS	129	VSS	217	DQ14_B	44	VSS	130	VSS	218	DQ15_B
45	DQ12_A	131	CK0_A_t	219	VSS	46	DQ13_A	132	CK1_A_t	220	VSS
47	VSS	133	CK0_A_c	221	DQ16_B	48	VSS	134	CK1_A_c	222	DQ17_B
49	DQ14_A	135	VSS	223	VSS	50	DQ15_A	136	VSS	224	VSS
51	VSS	137	CK0_B_t	225	DQ18_B	52	VSS	138	CK1_B_t	226	DQ19_B
53	DQ16_A	139	CK0_B_c	227	VSS	54	DQ17_A	140	CK1_B_c	228	VSS
55	VSS	141	VSS	229	DM2_B_n	56	VSS	142	VSS	230	DQS2_B_c
57	DQ18_A	143	RFU	231	VSS	58	DQ19_A	144	CA12_B	232	DQS2_B_t
59	VSS	145	CA11_B	233	DQ20_B	60	VSS	146	CA10_B	234	VSS
61	DM2_A_n	147	VSS	235	VSS	62	DQS2_A_c	148	VSS	236	DQ21_B
63	VSS	149	CA9_B	237	DQ22_B	64	DQS2_A_t	150	CA8_B	238	VSS
65	DQ20_A	151	CA7_B	239	VSS	66	VSS	152	CA6_B	240	DQ23_B
67	VSS	153	VSS	241	DQ24_B	68	DQ21_A	154	VSS	242	VSS
69	DQ22_A	155	CA5_B	243	VSS	70	VSS	156	CA4_B	244	DQ25_B
71	VSS	157	CA3_B	245	DQ26_B	72	DQ23_A	158	CA2_B	246	VSS
73	DQ24_A	159	VSS	247	VSS	74	VSS	160	VSS	248	DQ27_B
75	VSS	161	CS0_B_n	249	DQS3_B_c	76	DQ25_A	162	CA1_B	250	VSS
77	DQ26_A	163	RESET_n	251	DQS3_B_t	78	VSS	164	CA0_B	252	DM3_B_n
79	VSS	165	CS1_B_n	253	VSS	80	DQ27_A	166	VSS	254	VSS
81	DQS3_A_c	167	VSS	255	DQ28_B	82	VSS	168	CB0_B	256	DQ29_B
83	DQS3_A_t	169	DQS4_B_c	257	VSS	84	DM3_A_n	170	VSS	258	VSS
85	VSS	171	DQS4_B_t	259	DQ30_B	86	VSS	172	CB1_B	260	DQ31_B
87	DQ28_A	173	VSS	261	VSS	88	DQ29_A	174	VSS	262	VSS

Function Block Diagram

1Rank, x8 DDR5 SDRAMs



Note : ZQ resistors are 240Ω ± 1%.

Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Note
Operating Temperature	TOPER	0 to 85	°C	1,2

Note: Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on V_{DD} relative to Vss	VDD	-0.3 ~ 1.4	V	1
Voltage on V_{DDQ} pin relative to Vss	VDDQ	-0.3 ~ 1.4	V	1
Voltage on any pin relative to Vss	VIN, VOUT	-0.3 ~ 1.4	V	1
Storage temperature	T_{STG}	-55~+100	°C	1,2

Note:
1. Stress greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

AC & DC Operating Conditions

Recommended DC operating conditions

Parameter	Symbol	Voltage	Rating			Unit	Notes
			Min	Typ.	Max		
Host Supply Voltage	VIN_BULK	12.0	4.25	5.0	5.5	V	
PMIC Output Supply Voltage	VDD	1.1	1.067	1.1	1.166	V	1,2,3
PMIC Output Supply Voltage	VDDQ	1.1	1.067	1.1	1.166	V	1,2,3
PMIC Output Supply Voltage	VPP	1.8	1.746	1.8	1,908	V	3
AC Input Logic High	$V_{IH(AC)}$	TBD	-	-	-	mV	
AC Input Logic Low	$V_{IL(AC)}$	TBD	-	-	-	mV	
DC Input Logic High	$V_{IH(DC)}$	TBD	-	-	-	mV	
DC Input Logic Low	$V_{IL(DC)}$	TBD	-	-	-	mV	

Note: (1) VDD must be within 66mv of VDDQ
(2) AC parameters are measured with VDD and VDDQ tied together.
(3) This includes all voltage noise from DC to 2 MHz at the DRAM package ball.

IDD Specification parameters Definition - 16GB

Symbol	Condition	16GB	Unit
IDD0	One bank ACTIVATE-PRECHARGE current	530	mA
IDD0F	Operating Four Bank Active-Precharge Current	1000	mA
IDD2N	Precharge Standby Current	300	mA
IDD2P	Precharge Power-Down Current	230	mA
IDD3N	Active standby current	50	mA
IDD3P	Active Power-Down Current	300	mA
IDD4R	Burst Read Current	1900	mA
IDD4W	Burst write current	2300	mA
IDD5B	Burst Refresh Current (1x REF)	2300	mA
IDD5C	Burst Refresh Current (Same Bank Refresh Mode)	620	mA
IDD6N	Self refresh current: Normal temperature range (0–85°C)	3200	mA
IDD7	Bank interleave read current	160	mA
IDD8	Maximum power-down current	530	mA

■ Timing Parameters & Specifications

Parameter	Symbol	DDR5-4400		DDR5-4800		DDR5-5200		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Clock Timing									
Clock period average	tCK (AVG)	0.5	<0.500	0.4	<0.454	0.4	<0.416	ns	1
Command and Address Timing									
Read to Read command delay for same bank group	tCCD_L	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	nCK,ns	
Write to Write command delay for same bank groupp	tCCD_L_WR	max(32nCK, 20ns)	–	max(32nCK, 20ns)	–	max(32nCK, 20ns)	–	nCK,ns	
Write to Write command delay for same bank group, second write not RMW	tCCD_L_WR2	max(16nCK, 10ns)	–	max(16nCK, 10ns)	–	max(16nCK, 10ns)	–	nCK,ns	
Read to Write command delay for same bank group	tCCD_L_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3,5,6
Write to Read command delay for same bank group	tCCD_L_WTR	CWL + WBL/2 + Max(16nCK,10ns)						nCK,ns	4,6
Read to Read command delay for different bank group	tCCD_S	8	–	8	–	8	–	nCK	
Write to Write command delay for different bank group	tCCD_S_WR	8	–	8	–	8	–	nCK	
Read to Write command delay for different bank group	tCCD_S_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3,5,6
Write to Read command delay for different bank group	tCCD_S_WTR	CWL + WBL/2 + Max(4nCK,2.5ns)						nCK,ns	4,6
Write to Read with Auto Precharge command delay for same bank	tCCD_WTRA	CWL + WBL/2 + tWR - tRTP						nCK,ns	2,4,6

Parameter	Symbol	DDR5-4400		DDR5-4800		DDR5-5200		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Activate to Activate command delay to same bank group for 1KB page size	tRRD_L(1K)	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	nCK,ns	
Activate to Activate command delay to same bank group for 2KB page size	tRRD_L(2K)	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	nCK,ns	
Activate to Activate command delay to different bank group for 1KB page size	tRRD_S(1K)	8	–	8	–	8	–	nCK	
Activate to Activate command delay to different bank group for 2KB page size	tRRD_S(2K)	8	–	8	–	8	–	nCK	
Four activate window for 1KB page size	tFAW (1K)	Max(32nCK, 14.545ns)	–	Max(32nCK, 13.333ns)	–	Max(32nCK, 12.307ns)	–	nCK,ns	
Four activate window for 2KB page size	tFAW (2K)	Max(40nCK, 18.181ns)	–	Max(40nCK, 16.666ns)	–	Max(40nCK, 15.384ns)	–	nCK,ns	
Read to Precharge command delay	tRTP	Max(12nCK, 7.5ns)	–	Max(12nCK, 7.5ns)	–	Max(12nCK, 7.5ns)	–	nCK,ns	
Precharge to Precharge command delay	tPPD	2	–	2	–	2	–	nCK	7
Write recovery time	tWR	30	–	30	–	30	–	ns	

Notes:

1. tCK(avg)min listed for reference only, refer to the Speed Bins and Operations section which lists all valid tCK(avg) values.

2. tCCD_WTRA(min) shall always be greater than or equal to CWL + WBL/2 + tWR(min) - tRTP(min), and when using the appropriate rounding algorithms,

   nCCD_WTRA(min) shall always be greater than or equal to CWL + WBL/2 + nWR(min) - nRTP(min).

3. RBL: Read burst length associated with Read command

   RBL = 32 (36 w/ RCRC on) for fixed BL32 and BL32 in BL32 OTF mode

   RBL = 16 (18 w/ RCRC on) for fixed BL16 and BL16 in BL32 OTF mode

   RBL = 16 (18 w/ RCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode

4. WBL: Write burst length associated with Write command

   WBL = 32 (36 w/ WCRC on) for fixed BL32 and BL32 in BL32 OTF mode

   WBL = 16 (18 w/ WCRC on) for fixed BL16 and BL16 in BL32 OTF mode

   WBL = 16 (18 w/ WCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode

5. 5 - The following is considered for tRTW equation

   1tCK needs to be added due to tDQS2CK

   Read DQS offset timing can pull in the tRTW timing

   1tCK needs to be added when 1.5tCK postamble

6. CWL=CL-2

7. tPPD applies to any combination of precharge commands (PREab, PREsb, PREpb). tPPD also applies to any combination of precharge commands to a different die in a 3DS DDR5 SDRAM.

SERIAL PRESENCE DETECT SPECIFICATION

Byte	Function Described	Function		HEX Value
0	Number of Bytes in SPD Device	SPD Total: 1024Bytes		30
1	SPD Revision for Base Configuration Parameters	Version 1.0		10
2	Key Byte / Host Bus Command Protocol Type	DDR5 SDRAM		12
3	Key Byte / Module Type	SO-DIMM		03
4	First SDRAM Density and Package	Monolithic SDRAM	16Gb	04
5	First SDRAM Addressing	Row : 16	Column : 10	00
6	First SDRAM I/O Width	x8		20
7	First SDRAM Bank Groups & Banks Per Bank Group	8 bank groups/4 banks per bank group		62
8	Second SDRAM Density and Package			00
9	Second SDRAM Addressing			00
10	Secondary SDRAM I/O Width			00
11	Second SDRAM Bank Groups & Banks Per Bank Group			00
12	SDRAM BL32 & Post Package Repair	sPPR Undo/Lock supported	Burst length 32 supported	70
13	SDRAM Duty Cycle Adjuster & Partial Array Self Refresh	PASR/Device supports DCA for 4-phase internal clock(s)		00
14	SDRAM Fault Handling			00
15	Reserved	must be coded as 0x00		00
16	SDRAM Nominal Voltage, VDD	Operable:1.1V	Endurant:1.1V	00
17	SDRAM Nominal Voltage, VDDQ	Operable:1.1V	Endurant:1.1V	00
18	SDRAM Nominal Voltage, VPP	Operable:1.8V	Endurant:1.8V	00
19	SDRAM Timing	Standard core timings per JESD79-5		00
20	SDRAM Minimum Cycle Time (tCKAVGmin), Least Significant Byte	416 ps		A0
21	SDRAM Minimum Cycle Time (tCKAVGmin), Most Significant Byte			01
22	SDRAM Maximum Cycle Time (tCKAVGmax), Least Significant Byte	1010 ps		F2
23	SDRAM Maximum Cycle Time (tCKAVGmax), Most Significant Byte			03
24	SDRAM CAS Latencies Supported:First Byte	CL22,26,28,30,32		7A
25	SDRAM CAS Latencies Supported:Second Byte	CL36,40,42		0D
26	SDRAM CAS Latencies Supported:Third Byte	-		00
27	SDRAM CAS Latencies Supported:Fourth Byte	-		00
28	SDRAM CAS Latencies Supported:Fifth Byte	-		00
29	Reserved	must be coded as 0x00		00
30	SDRAM Minimum CAS Latency Time (tAAmin), Least Significant Byte	16000 ps		80
31	SDRAM Minimum CAS Latency Time (tAAmin), Most Significant Byte			3E
32	SDRAM Minimum RAS to CAS Delay Time (tRCDmin), Least Significant Byte	16000 ps		80
33	SDRAM Minimum RAS to CAS Delay Time (tRCDmin), Most Significant Byte			3E
34	SDRAM Minimum Row Precharge Delay Time (tRPmin), Least Significant Byte	16000 ps		80
35	SDRAM Minimum Row Precharge Delay Time (tRPmin), Most Significant Byte			3E
36	SDRAM Minimum Active to Precharge Delay Time (tRASmin), Least Significant Nibble	32000 ps		00
37	SDRAM Minimum Active to Precharge Delay Time (tRASmin), Most Significant Byte			7D
38	SDRAM Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Nibble	48000 ps		80
39	SDRAM Minimum Active to Active/Refresh Delay Time (tRCmin), Most Significant Nibble			BB
40	SDRAM Minimum Write Recovery Time (tWRmin), Least Significant Nibble	30000 ps		30
41	SDRAM Minimum Write Recovery Time (tWRmin), Most Significant Nibble			75
42	SDRAM Minimum Refresh Recovery Delay Time (tRFC1min, tRFC1_slr min),Least Significant Byte	295 ns		27
43	SDRAM Minimum Refresh Recovery Delay Time (tRFC1min, tRFC1_slr min),Most Significant Byte			01
44	SDRAM Minimum Refresh Recovery Delay Time (tRFC2min, tRFC2_slr min),Least Significant Byte	160 ns		A0
45	SDRAM Minimum Refresh Recovery Delay Time (tRFC2min, tRFC2_slr min),Most Significant Byte			00
46	SDRAM Minimum Refresh Recovery Delay Time (tRFCsbmin, tRFCsb_slr min),Least Significant Byte	130 ns		82
47	SDRAM Minimum Refresh Recovery Delay Time (tRFCsbmin, tRFCsb_slr min),Most Significant Byte			00
48	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFC1_dlr min),Least Significant Byte	monolithic SDRAMs,code as 0x00		00
49	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFC1_dlr min),Most Significant Byte			00
50	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFC2_dlr min),Least Significant Byte	monolithic SDRAMs,code as 0x00		00
51	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFC2_dlr min),Most Significant Byte			00
52	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFCsb_dlr min),Least Significant Byte	monolithic SDRAMs,code as 0x00		00
53	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFCsb_dlr min),Most Significant Byte			00
54	SDRAM Refresh Management, First Byte, First SDRAM			00
55	SDRAM Refresh Management, Second Byte, First SDRAM			00
56	SDRAM Refresh Management, First Byte, Second SDRAM			00
57	SDRAM Refresh Management, Second Byte, Second SDRAM			00
58	SDRAM Adaptive Refresh Management, First SDRAM, First Byte,Level A			00
59	SDRAM Adaptive Refresh Management, First SDRAM, Second Byte,Level A			00
60	SDRAM Adaptive Refresh Management, Second SDRAM, First Byte,Level A			00
61	SDRAM Adaptive Refresh Management, Second SDRAM, Second Byte,Level A			00
62	SDRAM Adaptive Refresh Management, First SDRAM, First Byte,Level B			00
63	SDRAM Adaptive Refresh Management, First SDRAM, Second Byte,Level B			00
64	SDRAM Adaptive Refresh Management, Second SDRAM, First Byte,Level B			00

65	SDRAM Adaptive Refresh Management, Second SDRAM, Second Byte,Level B			00
66	SDRAM Adaptive Refresh Management, First SDRAM, First Byte,Level C			00
67	SDRAM Adaptive Refresh Management, First SDRAM, Second Byte,Level C			00
68	SDRAM Adaptive Refresh Management, Second SDRAM, First Byte,Level C			00
69	SDRAM Adaptive Refresh Management, Second SDRAM, Second Byte,Level C			00
70	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group,(tRRD_Lmin),Least Significant Byte	5000	ps	88
71	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group,(tRRD_Lmin),Most Significant Byte			13
72	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group,(tRRD_Lmin),Lower Clock Limit	8	nCK	08
73	SDRAM Minimum CAS_n to CAS_n Command Delay Time, Same Bank Group,(tCCD_Lmin),Least Significant Byte	5000	ps	88
74	SDRAM Minimum CAS_n to CAS_n Command Delay Time, Same Bank Group,(tCCD_Lmin),Most Significant Byte			13
75	SDRAM Minimum CAS_n to CAS_n Command Delay Time, Same Bank Group,(tCCD_Lmin),Lower Clock Limit	8	nCK	08
76	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group (tCCD_L_WRmin),Least Significant Byte	20000	ps	20
77	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group (tCCD_L_WRmin),Most Significant Byte			4E
78	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group (tCCD_L_WRmin),Lower Clock Limit	32	nCK	20
79	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group (tCCD_L_WR2min),Least Significant Byte	10000	ps	10
80	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group (tCCD_L_WR2min),Most Significant Byte			27
81	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group (tCCD_L_WR2min),Lower Clock Limit	16	nCK	10
82	SDRAM Minimum Four Activate Window (tFAWmin),Least Significant Byte	13333	ps	15
83	SDRAM Minimum Four Activate Window (tFAWmin),Most Significant Byte			34
84	SDRAM Minimum Four Activate Window (tFAWmin),Lower Clock Limit	32	nCK	20
85	SDRAM Write to Read Command Delay for Same Bank Group (tCCD_L_WTR),Least Significant Byte	10000	ps	10
86	SDRAM Write to Read Command Delay for Same Bank Group (tCCD_L_WTR), Most Significant Byte			27
87	SDRAM Write to Read Command Delay for Same Bank Group (tCCD_L_WTR),Lower Clock Limit	16	nCK	10
88	SDRAM Write to Read Command Delay for Different Bank Group (tCCD_S_WTR), Least Significant Byte	2500	ps	C4
89	SDRAM Write to Read Command Delay for Different Bank Group (tCCD_S_WTR), Most Significant Byte			09
90	SDRAM Write to Read Command Delay for Different Bank Group,(tCCD_S_WTR), Lower Clock Limit	4	nCK	04
91	SDRAM Read to Precharge Command Delay (tRTP, tRTP_slr), Least Significant Byte	7500	ps	4C
92	SDRAM Read to Precharge Command Delay (tRTP, tRTP_slr), Most Significant Byte			1D
93	SDRAM Read to Precharge Command Delay (tRTP, tRTP_slr), Lower Clock Limit	12	nCK	0C
94-127	Reserved, Base Configuration Section	Must be coded as 0x00		00
128-191	Reserved for future use	Reserved for future use		00
192	SPD Revision for Module Information	Version 1.0		10
193	Hashing Sequence	No authentication		00
194	SPD Manufacturer ID Code, First Byte	By SPD_Hub & PMIC Vendor & Revision *Note: 1		-
195	SPD Manufacturer ID Code, Second Byte			-
196	SPD Device Type			-
197	SPD Device Revision Number			-
198	PMIC 0 Manufacturer ID Code, First Byte			-
199	PMIC 0 Manufacturer ID Code, Second Byte			-
200	PMIC 0 Device Type			-
201	PMIC 0 Revision Number			-
202	PMIC 1 Manufacturer ID Code, First Byte			00
203	PMIC 1 Manufacturer ID Code, Second Byte			00
204	PMIC 1 Device Type			00
205	PMIC 1 Revision Number			00
206	PMIC 2 Manufacturer ID Code, First Byte			00
207	PMIC 2 Manufacturer ID Code, Second Byte			00
208	PMIC 2 Device Type			00
209	PMIC 2 Revision Number			00
210	Thermal Sensor Manufacturer ID Code, First Byte			00
211	Thermal Sensor Manufacturer ID Code, Second Byte			00
212	Thermal Sensor Device Type			00
213	Thermal Sensor Revision Number			00
214	DRAM Specification Level			00
215	SPD Specification Level			00
216	PMIC0 Specification Level			00
217	PMIC1 Specification Level			00
218	PMIC2 Specification Level			00
219	TS Specification Level			00
220	DIMM Specification Level			00
221-229	Reserved	Reserved		00
230	(Unbuffered): Module Nominal Height	30mm		0F
231	(Unbuffered): Module Maximum Thickness	Front,1 < thickness < 2 mm		01
232	(Unbuffered): Reference Raw Card Used	Raw Card A	Revision 0	00
233	(Unbuffered): DIMM Attributes	0 to +95 °C/2 row DRAM		82
234	(Unbuffered): Module Organization	1 Package Ranks		00
235	Memory Channel Bus Width	2 channels/32 bits/ 4 bits ecc per bus		2A
236-239	Reserved	must be coded as 0x00		00
240~447	(Unbuffered):Module Type Specific Information	Reserved		00

448-509	Reserved for future use	-	**00**
510	CRC for Byte 0~509,Least Significant Byte	**CRC**	**-**
511	CRC for Byte 0~509,Most Significant Byte	**CRC**	**-**
512	Module Manufacturer ID Code, First Byte		**04**
513	Module Manufacturer ID Code, Second Byte		**CB**
514	Module Manufacturing Location	*Note: 2	**-**
515	Module Manufacturing Date	*Note: 3 (Decimal)	**-**
516	Module Manufacturing Date	*Note: 4 (Decimal)	**-**
517	Module Serial Number	*Note: 5 (Decimal)	**-**
518			**-**
519			**-**
520			**-**
521~550	Module Part Number	*Note: 6	**--**
551	Module Revision Code		**00**
552	DRAM Manufacturer ID Code, First Byte	*Note: 7	**-**
553	*DRAM* Manufacturer ID Code, Second Byte		**-**
554	DRAM Stepping	Undefined/Stepping information not provided	**FF**
555-639	Manufacturer's Specific Data	*Note: 8	**-**
640	Intel Extreme Memory Profile Identification String		**00**
641	Intel Extreme Memory Profile Identification String		**00**
642	Intel Extreme Memory Profile Version		**00**
643	Intel Extreme Memory Profile Organization		**00**
644	Intel Extreme Memory Profile Configuration		**00**
645	PMIC Vendor ID		**00**
646	PMIC Vendor ID		**00**
647	Number of PMICs		**00**
648	PMIC Capabilities		**00**
649-653	RSVD		**00**
654~701	Profile 1/2/3 String Name		**00**
702~895	Profile 1/2/3 Parameter		**00**
896-1023	User Settings		**00**

Note :

1. Byte 194-201 -- By SPD_Hub & PMIC Vendor & Revision
1.1 Byte 194-197 – RENESAS[(0x80), (0xB3), (0x80), (0x21)] ; MONTAGE[(0x86), (0x32), (0x80), (0x15)]
1.2 Byte 198-201 – RENESAS[(0x80), (0xB3), (0x82), (0x20)] ; RICHTEK[(0x8A), (0x8C), (0x82), (0x11)]
2. Byte 514 -- Manufacturing location by manufacturing location
3. Byte 515 -- Module manufacturing date by year (YY). (Decimal)
4. Byte 516 -- Module manufacturing date by week (WW). (Decimal)
5. Bytes 517-520 -- Module Serial Number. (Decimal)
6. Bytes 521-550 -- Module Part Number. (ASCII format, unused digits are coded as ASCII blanks (0x20).
7. Bytes 552-553 -- DRAM Manufacturer ID Code by JEDEC definition. SAMSUNG :[(0x80) ,(0xCE)]
8. Bytes 555~639 -- These bytes are undefined and can be used own purpose