Advantech

AQD-SD5V8GN56-SCH

Datasheet

Rev. 1.0

2024-04-01

Description

DDR5 1.1V SO-DIMM is high-speed, low power memory module that use 1Gx16 bits DDR5 SDRAM in FBGA package and a 8192 bits serial EEPROM on a 262-pin printed circuit board. DDR5 1.1V SO-DIMM is a Dual In-Line Memory Module and is intended for mounting into 262-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

- JEDEC standard compliant
- On-DIMM thermal sensor : Yes
- VDD = VDDQ= 1.1V (1.067V to 1.166V)
- VPP = 1.8V (1.746V to 1.908V)、VDDSPD = 1.8V
- 32 internal banks (x4, x8): 8 groups of 4 banks each
- 16 internal banks (x16): 4 groups of 4 banks each
- CAS Latency (CL): 22,26,28,30,32,36,40,42,46,48,50
- CAS Write Latency (CWL): RL-2
- Operating temperature Tcase–(0℃~85℃)
- Average Refresh period 3.9us at lower than Tcase 85°C, 1.95us at 85°C < Tcase < 95 °C.
- All bank and same bank refresh
- Bi-Directional Differential Data Strobe
- 16-bit prefetch architecture
- On-die ECC
- ECC transparency and error scrub
- sPPR and hPPR capability
- PCB: 30μ inch gold finger
- Halogen free、Lead-free (RoHS compliant)
- Anti-Sulfuration (Anti-FOS test: ASTM-B809-95)

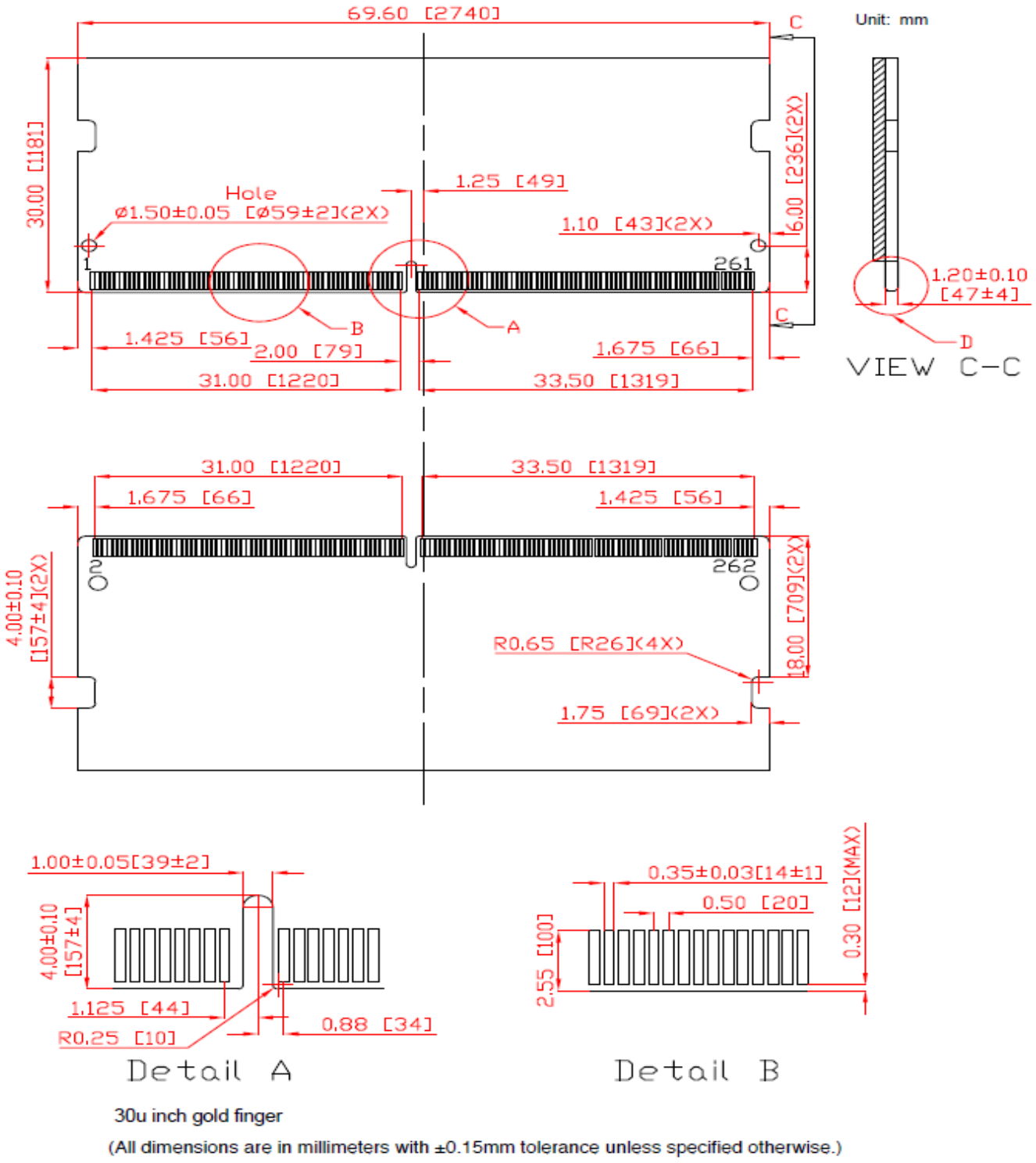
Pin Identification

Symbol	Function
CA0_A – CA12_A, CA0_B – CA12_B	SDRAM Command/Address bus
CS0_A_n – CS1_A_n, CS0_B_n – CS1_B_n	SDRAM Chip Select
DQ0_A – DQ31_A, DQ0_B – DQ31_B	DIMM memory data bus
CB0_A – CB3_A, CB0_B – CB3_B	DIMM ECC check bits (Only applicable on ECC SODIMM or ECC UDIMM)
DQS0_A_t – DQS4_A_t, DQS0_B_t – DQS4_B_t	SDRAM data strobes (positive line of differential pair)
DQS0_A_c – DQS4_A_c, DQS0_B_c – DQS4_B_c	SDRAM data strobes (negative line of differential pair)
DM0_A_n – DM3_A_n, DM0_B_n – DM3_B_n	SDRAM data masks
CK0_A_t, CK1_A_t, CK0_B_t, CK1_B_t	SDRAM clocks (positive line of differential pair)
CK0_A_c, CK1_A_c, CK0_B_c, CK1_B_c	SDRAM clocks (negative line of differential pair)
HSCL	Side Band bus clock
HSDA	Side Band bus data
HSA	Side Band bus address
ALERT_n	SDRAM ALERT_n
RESET_n	Set DRAMs to a Known State
VIN_BULK	5 V power input supply to the PMIC for analog circuits
VSS	Power supply return (ground)
PWR_GOOD	Power good indicator
PWR_EN	PMIC Enable
RFU	Reserved for future use

*Notes:
DDR5 SO-DIMM has 2 channels (channel-A and channel-B) of signal bus.

The signals with suffix: _A (e.g. DQ0_A) are for channel-A, and the signals with suffix: _B (e.g. DQ0_B) are for channel-B

Dimensions (Unit: millimeter)



30u inch gold finger

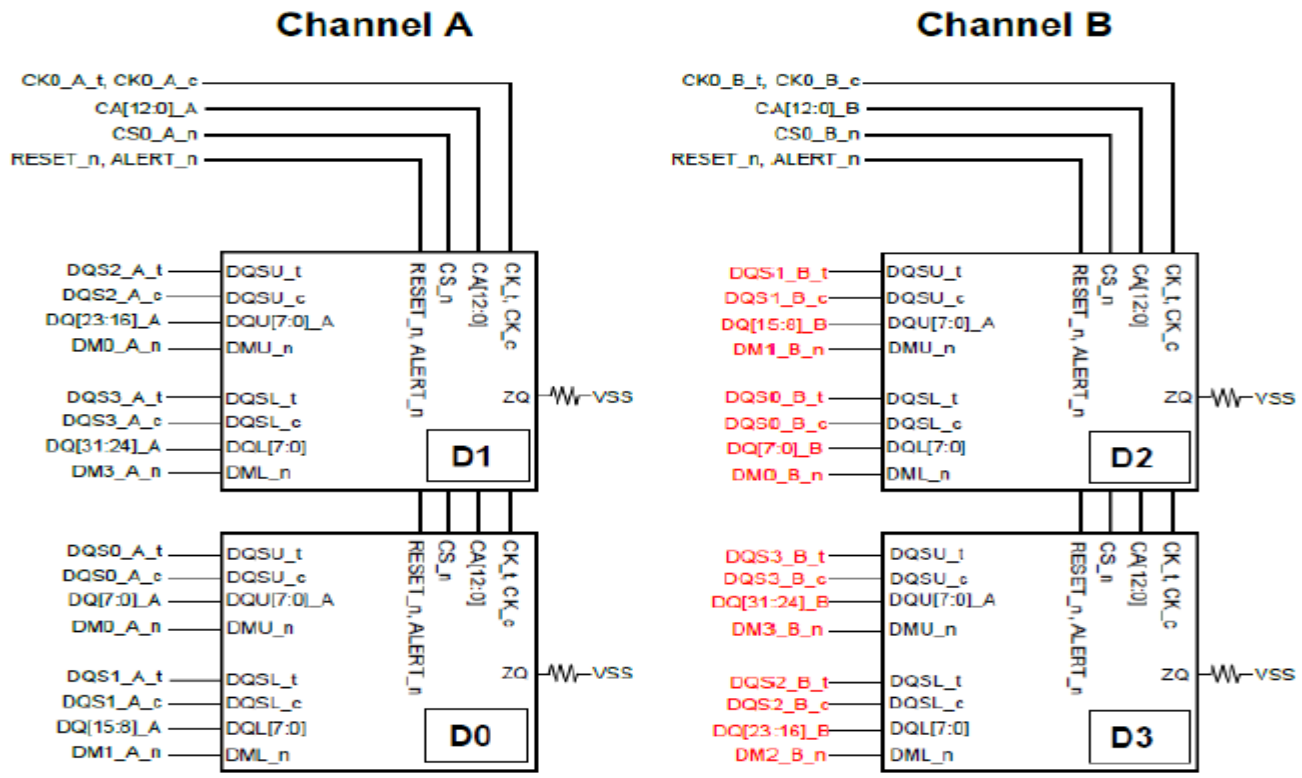
(All dimensions are in millimeters with ±0.15mm tolerance unless specified otherwise.)

Pin Assignments

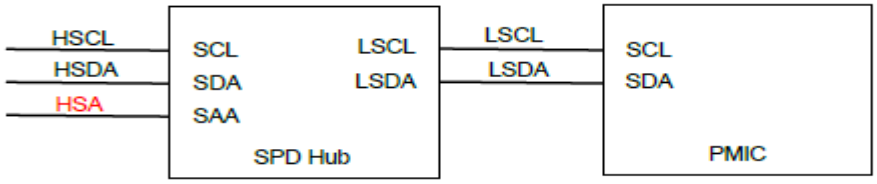
Pin No.	Front Side	Pin No.	Back Side	Pin No.	Front Side	Pin No.	Back Side
1	VIN_BULK	2	HSA	133	CK0_A_c	134	CK1_A_c
3	VIN_BULK	4	HSCL	135	VSS	136	VSS
5	RFU	6	HSDA	137	CK0_B_t	138	CK1_B_t
7	PWR_GOOD	8	PWR_EN	139	CK0_B_c	140	CK1_B_c
9	VSS	10	VSS	141	VSS	142	VSS
11	DQ0_A	12	DQ1_A	143	RFU	144	CA12_B
13	VSS	14	VSS	145	CA11_B	146	CA10_B
15	DQ2_A	16	DQ3_A	147	VSS	148	VSS
17	VSS	18	VSS	149	CA9_B	150	CA8_B
19	DM0_A_n	20	DQS0_A_c	151	CA7_B	152	CA6_B
21	VSS	22	DQS0_A_t	153	VSS	154	VSS
23	DQ4_A	24	VSS	155	CA5_B	156	CA4_B
25	VSS	26	DQ5_A	157	CA3_B	158	CA2_B
27	DQ6_A	28	VSS	159	VSS	160	VSS
29	VSS	30	DQ7_A	161	CS0_B_n	162	CA1_B
31	DQ8_A	32	VSS	163	RESET_n	164	CA0_B
33	VSS	34	DQ09_A	165	CS1_B_n	166	VSS
35	DQ10_A	36	VSS	167	VSS	168	CB0_B
37	VSS	38	DQ11_A	169	DQS4_B_c	170	VSS
39	DQS1_A_c	40	VSS	171	DQS4_B_t	172	CB1_B
41	DQS1_A_t	42	DM1_A_n	173	VSS	174	VSS
43	VSS	44	VSS	175	CB3_B	176	CB2_B
45	DQ12_A	46	DQ13_A	177	VSS	178	VSS
47	VSS	48	VSS	179	DQ0_B	180	DQ1_B
49	DQ14_A	50	DQ15_A	181	VSS	182	VSS
51	VSS	52	VSS	183	DQ2_B	184	DQ3_B
53	DQ16_A	54	DQ17_A	185	VSS	186	VSS
55	VSS	56	VSS	187	DM0_B_n	188	DQS0_B_c
57	DQ18_A	58	DQ19_A	189	VSS	190	DQS0_B_t
59	VSS	60	VSS	191	DQ4_B	192	VSS
61	DM2_A_n	62	DQS2_A_c	193	VSS	194	DQ5_B
63	VSS	64	DQS2_A_t	195	DQ6_B	196	VSS
65	DQ20_A	66	VSS	197	VSS	198	DQ7_B

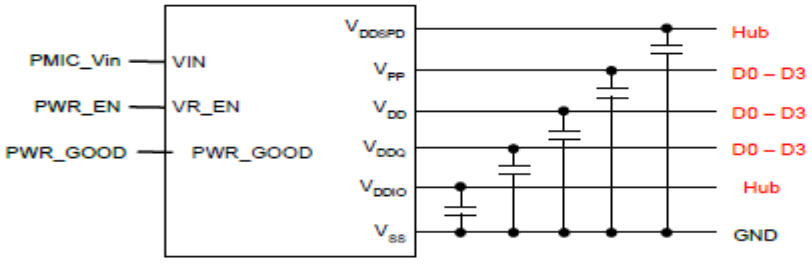
Pin No.	Front Side	Pin No.	Back Side	Pin No.	Front Side	Pin No.	Back Side
67	VSS	68	DQ21_A	199	DQ8_B	200	VSS
69	DQ22_A	70	VSS	201	VSS	202	DQ9_B
71	VSS	72	DQ23_A	203	DQ10_B	204	VSS
73	DQ24_A	74	VSS	205	VSS	206	DQ11_B
75	VSS	76	DQ25_A	207	DQS1_B_c	208	VSS
77	DQ26_A	78	VSS	209	DQS1_B_t	210	DM1_B_n
79	VSS	80	DQ27_A	211	VSS	212	VSS
81	DQS3_A_c	82	VSS	213	DQ12_B	214	DQ13_B
83	DQS3_A_t	84	DM3_A_n	215	VSS	216	VSS
85	VSS	86	VSS	217	DQ14_B	218	DQ15_B
87	DQ28_A	88	DQ29_A	219	VSS	220	VSS
89	VSS	90	VSS	221	DQ16_B	222	DQ17_B
91	DQ30_A	92	DQ31_A	223	VSS	224	VSS
93	VSS	94	VSS	225	DQ18_B	226	DQ19_B
95	CB0_A	96	CB1_A	227	VSS	228	VSS
97	VSS	98	VSS	229	DM2_B_n	230	DQS2_B_c
99	CB2_A	100	DQS4_A_c	231	VSS	232	DQS2_B_t
101	VSS	102	DQS4_A_t	233	DQ20_B	234	VSS
103	CB3_A	104	VSS	235	VSS	236	DQ21_B
105	VSS	106	CS0_A_n	237	DQ22_B	238	VSS
107	CA0_A	108	ALERT_n	239	VSS	240	DQ23_B
109	CA1_A	110	CS1_A_n	241	DQ24_B	242	VSS
111	VSS	112	VSS	243	VSS	244	DQ25_B
113	CA2_A	114	CA3_A	245	DQ26_B	246	VSS
115	CA4_A	116	CA5_A	247	VSS	248	DQ27_B
117	VSS	118	VSS	249	DQS3_B_c	250	VSS
119	CA6_A	120	CA7_A	251	DQS3_B_t	252	DM3_B_n
121	CA8_A	122	CA9_A	253	VSS	254	VSS
123	VSS	124	VSS	255	DQ28_B	256	DQ29_B
125	CA10_A	126	CA11_A	257	VSS	258	VSS
127	CA12_A	128	RFU	259	DQ30_B	260	DQ31_B
129	VSS	130	VSS	261	VSS	262	VSS
131	CK0_A_t	132	CK1_A_t	–	–	–	–

Block Diagram
8GB, 1Gx64 Module (1 Rank x16)



Note 1: Unless otherwise noted resistors are 15Ω ± 5%
Note 2: ZQ resistors are 240Ω ± 1%.
Note 3: CK1_[A:B]_t/c edge pin signals are each terminated with 33Ω ± 5% resistor to VSS.
Note 4: CS1_[A:B]_n edge pin signals are each terminated with 39Ω ± 5% resistor to VSS.





Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Note
Normal Operating Temperature	Toper normal	-20 to 85	°C	1,2,3,4
Extended Operating Temperature	Toper extended	85 to 95		1,2,3,4,5

Note:
1. All operating temperature symbols, ranges, acronyms are referred from JESD402-1.
2. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. All DDR5 SDRAMs are required to operate in NT and XT temperature ranges.
4. If TC exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 1.95µs interval refresh rate.
5. Operating Temperature for 3DS needs to be derated by the number of DRAM dies as: [TOPER – (2.5°C × log2N)], where N is the number of the stacked dies.

Absolute Maximum DC Ratings

Parameter	Symbol	Rating	Units	Notes
Voltage on VDD pin relative to Vss	VDD	- 0.3 ~ 1.4	V	1
Voltage on VDDQ pin relative to Vss	VDDQ	- 0.3 ~ 1.4	V	1
Voltage on VPP pin relative to Vss	VPP	- 0.3 ~ 2.1	V	
Voltage on any pin relative to Vss	VIN, VOUT	- 0.3 ~ 1.4	V	1
Storage temperature	TSTG	– 55 to +100	°C	1,2

Note:
1. Stresses greater than those listed in this table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage temperature is the case surface temperature on the center/top side of the device. For the measurement conditions, refer to JESD51-2 standard.

AC & DC Operating Conditions

DIMM Voltage Requirements

Symbol	Parameter	Voltage Rating (Volts)			Maximum Expected Current (Amps)	Power State
		Minimum	Typical	Maximum		
VIN_BULK	Host Supply Voltage	4.25	5.0	5.5	2.A	Operational
SWA,SWB	PMIC Output Supply Voltage	-	1.1	-	Note 9	Operational
SWA+SWB	PMIC Output Supply Voltage	-	1.1	-	Note 9	Operational
SWC	PMIC Output Supply Voltage	-	1.8	-	Note 9	Operational
1.8V LDO	PMIC Output Supply Voltage	-	1.8	-	0.025(maximum)	Operational
1.0V LDO	PMIC Output Supply Voltage	-	1.0	-	0.020(maximum)	Operational

NOTE:
1. Input supplies referenced in this table are VIN_BULK and VIN.
2. During first power-on, the input voltage supply must reach a minimum of 4.25V for the PMIC to detect a valid input supply.
3. The ramp up rate is between 300mV and 4.0V.
4. The ramp down rate is between 4.0V and 300mV.
5. The area under the curve and above VIN_Bulk = TBD. The VIN_Bulk_AC spec must also be satisfied.
6. The minimum input current requirement is equal to the maximum output current on VOUT_1.8V and VOUT_1.0V LDO, plus the current required by the PMIC for its own use. The maximum input current is equal to the all VIN_Bulk input on the PMIC.
7. VIN_Bulk = 5.0V measured at room temperature. All circuitry, including output regulators and LDOs are off. The VR_EN

signal is static LOW or HIGH. The GSI_n signal is pulled HIGH. I2C or 13C basic interface access is not allowed, and the bus is pulled HIGH. The PID signal is pulled either HIGH or LOW

8. VIN_Bulk = 5.0V measured at room temperature. All output regulators and LDOs are on the 0A output load. The VR_EN signal is static LOW or HIGH. The GSI_n signal is pulled HIGH. I2C or 13C basic interface access is not allowed, and the bus is pulled HIGH. The PID signal is pulled either HIGH or LOW.
9. Maximum and Minimum Current ratings depend on PMIC (5100)

ADVANTECH

Enabling an Intelligent Planet

262 Pin DDR5 1.1V 5600 SO-DIMM
8GB Based on 1Gx16
AQD-SD5V8GN56-SCH

SERIAL PRESENCE DETECT SPECIFICATION

8192MB(1024Mx64Bit) Serial Presence Detect for DDR5 SODIMM (PC-44800) 5600 CL=46-45-45

BYTE	FUNCTION DESCRIDED	FUNCTION SUPPORTED	HEX VALUE
0	Number of Bytes in SPD Device	1024 bytes	30
1	SPD Revision for Base Configuration Parameters	Revision 1.0	10
2	Key Byte / Host Bus Command Protocol Type	DDR5 SDRAM	12
3	Key Byte / Module Type	SODIMM	03
4	First SDRAM Density and Package	Monolithic SDRAM, 16Gb	04
5	First SDRAM Addressing	16 rows, 10 columns	00
6	First SDRAM I/O Width	x16	40
7	First SDRAM Bank Groups & Banks Per Bank Group	4 bank groups, 4 banks per bank group	42
8	Second SDRAM Density and Package	Symmetrical	00
9	Second SDRAM Addressing	Symmetrical	00
10	Second SDRAM I/O Width	Symmetrical	00
11	Second SDRAM Bank Groups & Banks Per Bank Group	Symmetrical	00
12	SDRAM BL32 & Post Package Repair	One repair element per bank,Burst length 32 supported	90
13	SDRAM Duty Cycle Adjuster & Partial Array Self Refresh	Device supports DCA for 4-phase internal clocks	02
14	SDRAM Fault Handling	Bounded Fault supported,	00
15	RESERVED	must be coded as 00	00
16	SDRAM Nominal Voltage, VDD	1.1V	00
17	SDRAM Nominal Voltage, VDDQ	1.1V	00
18	SDRAM Nominal Voltage, VPP	1.8V	00
19	SDRAM Timing	SDRAM uses standard core timings per JESD79-5	00
20	SDRAM Minimum Cycle Time (tCKAVGmin) LSB	0.357ns	65
21	SDRAM Minimum Cycle Time (tCKAVGmin) MSB	0.357ns	01
22	SDRAM Maximum Cycle Time (tCKAVGmax), LSB	1.010ns	F2
23	SDRAM Maximum Cycle Time (tCKAVGmax), MSB	1.010ns	03
24	CAS Latencies Supported, First Byte	50,46,42,40,36,32,30,28,26,22	7A
25	CAS Latencies Supported, Second Byte	50,46,42,40,36,32,30,28,26,22	AD
26	CAS Latencies Supported, Third Byte	50,46,42,40,36,32,30,28,26,22	00

27	CAS Latencies Supported, Fourth Byte	50,46,42,40,36,32,30,28,26,22	00
28	CAS Latencies Supported, Fifth Byte	50,46,42,40,36,32,30,28,26,22	00
29	RESERVED	must be coded as 00	00
30	SDRAM Minimum CAS Latency Time (tAAmin), LSB	16.000	80
31	SDRAM Minimum CAS Latency Time (tAAmin), MSB	16.000	3E
32	SDRAM Minimum RAS to CAS Delay Time (tRCDmin), LSB	16.000	80
33	SDRAM Minimum RAS to CAS Delay Time (tRCDmin), MSB	16.000	3E
34	SDRAM Minimum Row Precharge Delay Time (tRPmin), LSB	16.000	80
35	SDRAM Minimum Row Precharge Delay Time (tRPmin), MSB	16.000	3E
36	SDRAM Minimum Active to Precharge Delay Time (tRASmin), LSB	32.000	00
37	SDRAM Minimum Active to Precharge Delay Time (tRASmin), MSB	32.000	7D
38	SDRAM Minimum Active to Active/Refresh Delay Time (tRCmin), LSB	48.000	80
39	SDRAM Minimum Active to Active/Refresh Delay Time (tRCmin), MSB	48.000	BB
40	SDRAM Minimum Write Recovery Time (tWRmin), LSB	30.000	30
41	SDRAM Minimum Write Recovery Time (tWRmin), MSB	30.000	75
42	SDRAM Minimum Refresh Recovery Delay Time (tRFC1min, tRFC1_slr min), LSB	295	27
43	SDRAM Minimum Refresh Recovery Delay Time (tRFC1min, tRFC1_slr min), MSB	295	01
44	SDRAM Minimum Refresh Recovery Delay Time (tRFC2min, tRFC2_slr min), LSB	160	A0
45	SDRAM Minimum Refresh Recovery Delay Time (tRFC2min, tRFC2_slr min), MSB	160	00
46	SDRAM Minimum Refresh Recovery Delay Time (tRFCsbmin, tRFCsb_slr min), LSB	130	82
47	SDRAM Minimum Refresh Recovery Delay Time (tRFCsbmin, tRFCsb_slr min), MSB	130	00
48	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFC1_dlr min), LSB	must be coded as 00	00
49	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFC1_dlr min), MSB	must be coded as 00	00
50	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFC2_dlr min), LSB	must be coded as 00	00
51	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFC2_dlr min), MSB	must be coded as 00	00
52	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFCsb_dlr min), LSB	must be coded as 00	00
53	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFCsb_dlr min), MSB	must be coded as 00	00
54	SDRAM Refresh Management, First Byte, First SDRAM	Refresh management not required	00
55	SDRAM Refresh Management, Second Byte, First SDRAM	Refresh management not required	00
56	SDRAM Refresh Management, First Byte, Second SDRAM	Refresh management not required	00

57	SDRAM Refresh Management, Second Byte, Second SDRAM	Refresh management not required	00
58	SDRAM Adaptive Refresh Management Level A, First Byte, First SDRAM	Adaptive refresh management not required	00
59	SDRAM Adaptive Refresh Management Level A, Second Byte, First SDRAM	Adaptive refresh management not required	00
60	SDRAM Adaptive Refresh Management Level A, First Byte, Second SDRAM	Adaptive refresh management not required	00
61	SDRAM Adaptive Refresh Management Level A, Second Byte, Second SDRAM	Adaptive refresh management not required	00
62	SDRAM Adaptive Refresh Management Level B, First Byte, First SDRAM	Adaptive refresh management not required	00
63	SDRAM Adaptive Refresh Management Level B, Second Byte, First SDRAM	Adaptive refresh management not required	00
64	SDRAM Adaptive Refresh Management Level B, First Byte, Second SDRAM	Adaptive refresh management not required	00
65	SDRAM Adaptive Refresh Management Level B, Second Byte, Second SDRAM	Adaptive refresh management not required	00
66	SDRAM Adaptive Refresh Management Level C, First Byte, First SDRAM	Adaptive refresh management not required	00
67	SDRAM Adaptive Refresh Management Level C, Second Byte, First SDRAM	Adaptive refresh management not required	00
68	SDRAM Adaptive Refresh Management Level C, First Byte, Second SDRAM	Adaptive refresh management not required	00
69	SDRAM Adaptive Refresh Management Level C, Second Byte, Second SDRAM	Adaptive refresh management not required	00
70	SDRAM Activate to Activate Command Delay for Same Bank Group (tRRD_L), Least Significant Byte	5000ps	88
71	SDRAM Activate to Activate Command Delay for Same Bank Group (tRRD_L), Most Significant Byte	5000ps	13
72	SDRAM Activate to Activate Command Delay for Same Bank Group (tRRD_L), Lower Clock Limit	8CK	08
73	SDRAM Read to Read Command Delay for Same Bank Group (tCCD_L), Least Significant Byte	5000ps	88
74	SDRAM Read to Read Command Delay for Same Bank Group (tCCD_L), Most Significant Byte	5000ps	13
75	SDRAM Read to Read Command Delay for Same Bank Group (tCCD_L), Lower Clock Limit	8CK	08
76	SDRAM Write to Write Command Delay for Same Bank Group (tCCD_L_WR), Least Significant Byte	20000ps	20
77	SDRAM Write to Write Command Delay for Same Bank Group (tCCD_L_WR), Most Significant Byte	20000ps	4E
78	SDRAM Write to Write Command Delay for Same Bank Group (tCCD_L_WR), Lower Clock Limit	32CK	20
79	SDRAM Write to Write Command Delay for Same Bank Group, Second Write not RMW (tCCD_L_WR2), Least Significant Byte	10000ps	10
80	SDRAM Write to Write Command Delay for Same Bank Group, Second Write not RMW (tCCD_L_WR2), Most Significant Byte	10000ps	27
81	SDRAM Write to Write Command Delay for Same Bank Group, Second Write not RMW (tCCD_L_WR2), Lower Clock Limit	16CK	10
82	SDRAM Four Activate Window (tFAW), Least Significant Byte	14285ps	CD
83	SDRAM Four Activate Window (tFAW), Most Significant Byte	14285ps	37
84	SDRAM Four Activate Window (tFAW), Lower Clock Limit	40CK	28
85	SDRAM Write to Read Command Delay for Same Bank Group (tCCD_L_WTR), Least Significant Byte	10000ps	10
86	SDRAM Write to Read Command Delay for Same Bank Group (tCCD_L_WTR), (tCCD_L_WTR), Most Significant Byte	10000ps	27

87	SDRAM Write to Read Command Delay for Same Bank Group (tCCD_L_WTR), Lower Clock Limit	16CK	10
88	SDRAM Write to Read Command Delay for Different Bank Group (tCCD_S_WTR), Least Significant Byte	2500ps	C4
89	SDRAM Write to Read Command Delay for Different Bank Group (tCCD_S_WTR), Most Significant Byte	2500ps	09
90	SDRAM Write to Read Command Delay for Different Bank Group, (tCCD_S_WTR), Lower Clock Limit	4CK	04
91	SDRAM Read to Precharge Command Delay (tRTP, tRTP_slr), Least Significant Byte	7500ps	4C
92	SDRAM Read to Precharge Command Delay (tRTP, tRTP_slr), Most Significant Byte	7500ps	1D
93	SDRAM Read to Precharge Command Delay (tRTP, tRTP_slr), Lower Clock Limit	12CK	0C
94-191	RESERVED	must be coded as 00	00
192	SPD Revision for Module Information	Revision 1.0	10
193	RESERVED		00
194	SPD Manufacturer ID Code, First Byte	installed	00
195	SPD Manufacturer ID Code, Second Byte	installed	00
196	SPD Device Type	installed	00
197	SPD Device Revision Number	installed	00
198	PMIC 0 Manufacturer ID Code, First Byte	installed	00
199	PMIC 0 Manufacturer ID Code, Second Byte	installed	00
200	PMIC 0 Device Type	installed	00
201	PMIC 0 Revision Number	installed	00
202	PMIC 1 Manufacturer ID Code, First Byte	Not installed	00
203	PMIC 1 Manufacturer ID Code, Second Byte	Not installed	00
204	PMIC 1 Device Type	Not installed	00
205	PMIC 1 Revision Number	Not installed	00
206	PMIC 2 Manufacturer ID Code, First Byte	Not installed	00
207	PMIC 2 Manufacturer ID Code, Second Byte	Not installed	00
208	PMIC 2 Device Type	Not installed	00
209	PMIC 2 Revision Number	Not installed	00
210	Thermal Sensors Manufacturer ID Code, First Byte	Not installed	00
211	Thermal Sensors Manufacturer ID Code, Second Byte	Not installed	00
212	Thermal Sensors Device Type	Not installed	00
213	Thermal Sensors Revision Number	Not installed	00

214-229	RESERVED		00
230	Module Nominal Height	30mm	0F
231	Module Maximum Thickness	1.2mm	11
232	Reference Raw Card Used	C0	02
233	DIMM Attributes	NT, Heat spreader not installed, 1 row	81
234	Module Organization	Symmetrical, 1 PKG Rank	00
235	Memory Channel Bus Width	2 channels, 0 bits, 32 bits	22
236	RESERVED		00
237	RESERVED		00
238	RESERVED		00
239	RESERVED		00
240	RESERVED	Not installed	00
241	RESERVED	Not installed	00
242	RESERVED	Not installed	00
243	RESERVED	Not installed	00
244	RESERVED	Not installed	00
245	RESERVED	Not installed	00
246	RESERVED	Not installed	00
247	RESERVED	Not installed	00
248	RESERVED	must be coded as 00	00
249	RESERVED	must be coded as 00	00
250	RESERVED	must be coded as 00	00
251	RESERVED	must be coded as 00	00
252	RESERVED	must be coded as 00	00
253	RESERVED	must be coded as 00	00
254	RESERVED	must be coded as 00	00
255	RESERVED	must be coded as 00	00
256	RESERVED	must be coded as 00	00
257-509	RESERVED		00
510	CRC for SPD bytes 0~509	CRC cover 0~509 byte	0C
511	CRC for SPD bytes 0~509	CRC cover 0~509 byte	5F

512	Module Manufacturer ID Code, First Byte	Advantech	8A
513	Module Manufacturer ID Code, Second Byte	Advantech	C8
514	Module Manufacturing Location	Variable	00
515	Module Manufacturing Date	Variable	00
516	Module Manufacturing Date	Variable	00
517	Module Serial Number	Variable	00
518	Module Serial Number	Variable	00
519	Module Serial Number	Variable	00
520	Module Serial Number	Variable	00
521	Module Part Number	A	41
522	Module Part Number	Q	51
523	Module Part Number	D	44
524	Module Part Number	-	2D
525	Module Part Number	S	53
526	Module Part Number	D	44
527	Module Part Number	5	35
528	Module Part Number	V	56
529	Module Part Number	8	38
530	Module Part Number	G	47
531	Module Part Number	N	4E
532	Module Part Number	5	35
533	Module Part Number	6	36
534	Module Part Number	-	2D
535	Module Part Number	S	53
536	Module Part Number	C	43
537	Module Part Number	H	48
538	Module Part Number	Blank Space	20
539	Module Part Number	Blank Space	20
540	Module Part Number	Blank Space	20
541	Module Part Number	Blank Space	20
542	Module Part Number	Blank Space	20
543	Module Part Number	Blank Space	20
544	Module Part Number	Blank Space	20
545	Module Part Number	Blank Space	20
546	Module Part Number	Blank Space	20
547	Module Part Number	Blank Space	20
548	Module Part Number	Blank Space	20
549	Module Part Number	Blank Space	20
550	Module Part Number	Blank Space	20
551	Module Revision Code	Revision 0	00
552	DRAM Manufacturer's ID Code, First Byte	Variable	00
553	DRAM Manufacturer's ID Code, Second Byte	Variable	00
554	DRAM Stepping	Undefined	FF
555-637	Module Manufacturer's Specific Data		00

638-1023	RESERVED		00