RoHS Compliant

Solid State Drive

SMI-Sxxx-AC Product Specifications for Advantech

June 1, 2026

Version 1.2

Specifications Overview:

- **Compliance with SATA Revision 3.2**
  - SATA 6 Gb/s interface
  - Backward compatible with SATA 1.5/3 Gb/s interfaces
- **Capacity**
  - 128, 256, 512 GB
  - 1 TB
- **Performance**[1]
  - Burst read/write: 600 MB/sec
  - Sequential read: Up to 550 MB/sec
  - Sequential write: Up to 480 MB/sec
  - Random read (4K): Up to 90,000 IOPS
  - Random write (4K): Up to 70,000 IOPS
- **Flash Management**
  - Low-Density Parity-Check (LDPC) Code
  - Bad Block Management
  - Global Wear Leveling
  - Flash Translation Layer: Page Mapping
  - Power Failure Management
  - ATA Secure Erase
  - TRIM
  - Hyper Cache Technology
  - S.M.A.R.T.
- **NAND Flash Type:** 3D TLC
- **MTBF:** >2,000,000 hours
- **Endurance**
  - 128 GB: 70 TBW
  - 256 GB: 200 TBW
  - 512 GB: 400 TBW
  - 1 TB: 800 TBW
- **Temperature Range**
  - Operating (Tc): 0°C to 70°C
  - Storage (Ta): -40°C to 70°C
- **Supply Voltage**
  - 5V ± 10%
- **Power Consumption**[1]
  - Active mode (Max.):1,375 mW
  - Idle mode: 450 mW
- **Connector Type**
  - 7-pin SATA signal connector
  - 15-pin SATA power connector
- **Physical Characteristics**
  - Form factor: 2.5”
  - Dimensions: 99.90 x 69.90 x 6.90, unit: mm
  - Plastic housing
- **RoHS Compliant**
- **Warranty: 3 years or TBW (whichever occurs first)**

Note:

1. Varies from capacities. The values for performance and power consumption presented are typical and may vary depending on flash configurations or platform settings. The term idle refers to the standby state of the device.

Table of Contents

1. Product Specifications 3

1.1 Performance 3
1.2 Environmental Specifications 3
1.3 Mean Time Between Failures (MTBF) 3
1.4 Endurance 4
1.5 Certification and Compliance 4

2. Pin Assignments 5

3. Flash Management 7

3.1 Error Correction/Detection 7
3.2 Bad Block Management 7
3.3 Global Wear Leveling 7
3.4 Flash Translation Layer – Page Mapping 7
3.5 Power Failure Management 8
3.6 ATA Secure Erase 8
3.7 TRIM 8
3.8 Hyper Cache Technology 8

4. Electrical Specifications 9

4.1 Operating Voltage 9
4.2 Power Consumption 9

5. Mechanical Specifications 10

6. Product Ordering Information 11

Appendix: Label Specifications 12

1. Product Specifications

1.1 Performance

Table 1-1 Performance Specifications

Capacity / Performance	128 GB	256 GB	512 GB	1 TB
Sequential Read (MB/s)	550	550	550	550
Sequential Write (MB/s)	480	480	480	480
4K Random Read (IOPS)	28,000	54,000	88,000	90,000
4K Random Write (IOPS)	70,000	70,000	70,000	67,000

Notes:
- Results may differ from various flash configurations or host system setting.
- Sequential read/write is based on CrystalDiskMark 8.0.4 with file size 1,000MB.
- Random read/write is measured using IOMeter with Queue Depth 32.

1.2 Environmental Specifications

Table 1-2 Environmental Specifications

Parameter	Type	Specifications
Temperature	Operating (Tc)	0°C to 70°C
	Non-operating (Ta)	-40°C to 70°C
Vibration	Non-operating	20G, 20~2000 Hz/random
Shock	Non-operating	1,500G/0.5ms, half-sine wave

Notes:
- This Environmental Specification table indicates the conditions for testing the device. Real world usages may affect the results.
- Tc: case temperature; Ta: ambient temperature. The operating temperature is determined by the case temperature. Adequate airflow is advisable as it enables the device to maintain optimal temperatures, especially in environments with heavy workloads.

1.3 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in SMI-Sxxx-AC . The prediction result for SMI-Sxxx-AC is more than 2,000,000 hours.

1.4 Endurance

The endurance of a storage device is predicted by TeraBytes Writte based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

Table 1-3 Endurance Specifications

Capacity	TeraBytes Written
128 GB	70
256 GB	200
512 GB	400
1 TB	800

Notes:

- The endurance of SSD could be estimated based on users' behaviors, NAND endurance cycles, and write amplification factor. It is not guaranteed by the flash vendor.
- TBW may vary from flash configuration and platform.
- The endurance test is based on JEDEC 218A & JEDEC 219A client workload.
- DWPD (Drive Writes Per Day) is calculated based on the number of times that user overwrites the entire capacity of an SSD per day of its lifetime during the warranty period. (3D NAND TLC warranty: 3 years)

1.5 Certification and Compliance

SMI-Sxxx-AC complies with the following standards:

- CE
- UKCA
- FCC
- RoHS

2. Pin Assignments

Table 2-1 describes the signal segment, and Table 2-2, power segment.

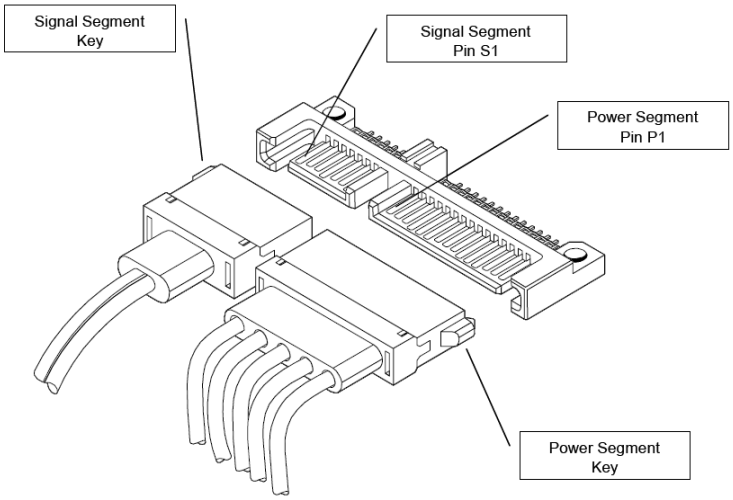

Figure 2-1 SATA Connectors

Table 2-1 Signal Segment

Pin	Type	Description
S1	GND	2nd mate
S2	A+	Differential signal A from Phy
S3	A-	
S4	GND	2nd mate
S5	B+	Differential signal B from Phy
S6	B-	
S7	GND	2nd mate

Table 2-2 Power Segment

Pin	Type	Description
P1	V33	3.3V power (Unused)
P2	V33	3.3V power (Unused)
P3	V33	3.3V power, pre charge, 2nd mate (Unused)
P4	GND	1st mate
P5	GND	2nd mate
P6	GND	2nd mate
P7	V5	5V power, pre charge, 2nd mate
P8	V5	5V power
P9	V5	5V power
P10	GND	2nd mate
P11	DAS/DSS	Device Activity Signal/Disable Staggered Spinup
P12	GND	1st mate
P13	V12	12V power, pre charge, mate (Unused)
P14	V12	12V power (Unused)

Pin	Type	Description
P15	V12	12V power (Unused)

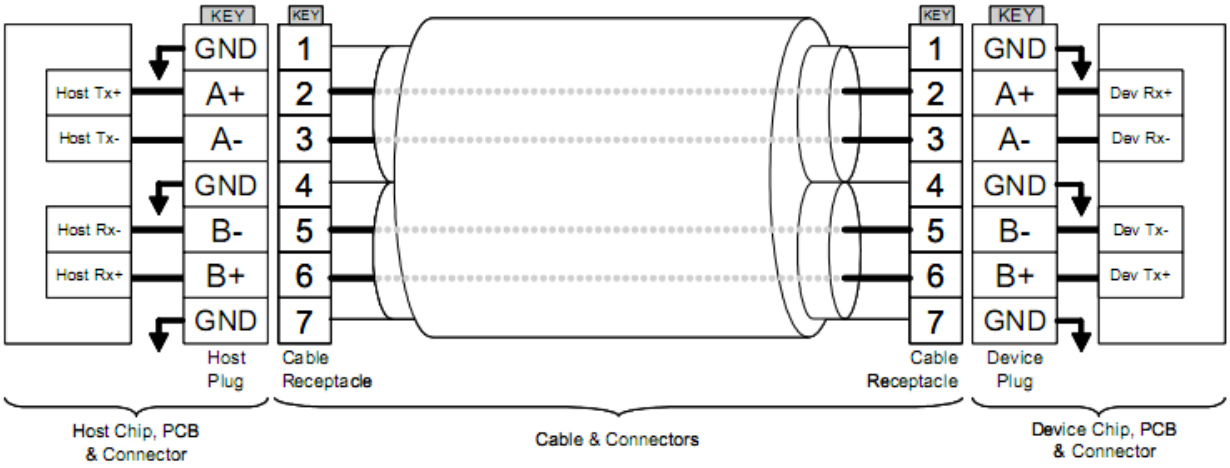

Figure 2-2 SATA Cable/Connector Connection Diagram

The connector on the left represents the Host with TX/RX differential pairs connected to a cable. The connector on the right shows the Device with TX/RX differential pairs also connected to the cable. Notice also the ground path connecting the shielding of the cable to the Cable Receptacle.

3. Flash Management

3.1 Error Correction/Detection

SMI-Sxxx-AC implements a hardware ECC scheme, based on the Low Density Parity Check (LDPC). LDPC is a class of linear block error correcting code which has apparent coding gain over BCH code because LDPC code includes both hard decoding and soft decoding algorithms. With the error rate decreasing, LDPC can extend SSD endurance and increase data reliability while reading raw data inside a flash chip.

3.2 Bad Block Management

Current production technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a minimal number of initial bad blocks during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. In addition, bad blocks may develop during program/erase cycles. Since bad blocks are inevitable, the solution is to keep them in control. The flash devices are programmed with ECC, page mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

3.3 Global Wear Leveling

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Global wear leveling is an important mechanism that levels out the wearing of all blocks so that the wearing-down of all blocks can be almost evenly distributed. This will increase the lifespan of SSDs.

3.4 Flash Translation Layer – Page Mapping

Page mapping is an advanced flash management technology whose essence lies in the ability to gather data, distribute the data into flash pages automatically, and then schedule the data to be evenly written. Page-level mapping uses one page as the unit of mapping. The most important characteristic is that each logical page can be mapped to any physical page on the flash memory device. This mapping algorithm allows different sizes of data to be written to a block as if the data is written to a data pool and it does not need to take extra operations to process a write command. Thus, page mapping is adopted to increase random access speed and improve SSD lifespan, reduce block erase frequency, and achieve optimized performance and lifespan.

3.5 Power Failure Management

Power Failure Management plays a crucial role when power supply becomes unstable. Power disruption may occur when users are storing data into the SSD, leading to instability in the drive. However, with Power Failure Management, a firmware protection mechanism will be activated to scan pages and blocks once power is resumed. Valid data will be transferred to new blocks for merging and the mapping table will be rebuilt. Therefore, data reliability can be reinforced, preventing damage to data stored in the NAND Flash.

3.6 ATA Secure Erase

ATA Secure Erase is an ATA disk purging command currently embedded in most of the storage drives. Defined in ATA specifications, (ATA) Secure Erase is part of Security Feature Set that allows storage drives to erase all user data areas. The erase process usually runs on the firmware level as most of the ATA-based storage media currently in the market are built-in with this command. ATA Secure Erase can securely wipe out the user data in the drive and protects it from malicious attack.

3.7 TRIM

TRIM is a SATA command that helps improve the read/write performance and efficiency of solid-state drives (SSD). The command enables the host operating system to inform SSD controller which blocks contain invalid data, mostly because of the erase commands from host. The invalid will be discarded permanently and the SSD will retain more space for itself.

3.8 Hyper Cache Technology

The proprietary Hyper Cache technology uses a portion of the available capacity as SLC (1bit-per-cell) NAND flash memory, called Hyper cache mode. When data is written to SSD, the firmware will direct the data to Hyper Cache mode, providing excellent performance to handle various scenarios in industrial use.

4. Electrical Specifications

4.1 Operating Voltage

Table 4-1 Operating Range

Item	Range
Supply Voltage	5V ± 10%

4.2 Power Consumption

Table 4-2 Power Consumption

Capacity / Mode	Unit	128 GB	256 GB	512 GB	1 TB
Active (Max.)	mW	1,075	1,100	1,125	1,375
Idle		450	450	450	450

Notes:

- All values are typical and may vary depending on flash configurations or host system settings.
- Power consumption is measured using CrystalDiskMark 8.0.4 with file size 1,000MB

5. Mechanical Specifications

Table 5-1 Physical Dimensions

Parameter	Unit	128 GB	256 GB	512 GB	1 TB
Length	mm	100.20 ± 0.25			
Width		69.85 ± 0.25			
Height		7.00 +0.20/-0.50			

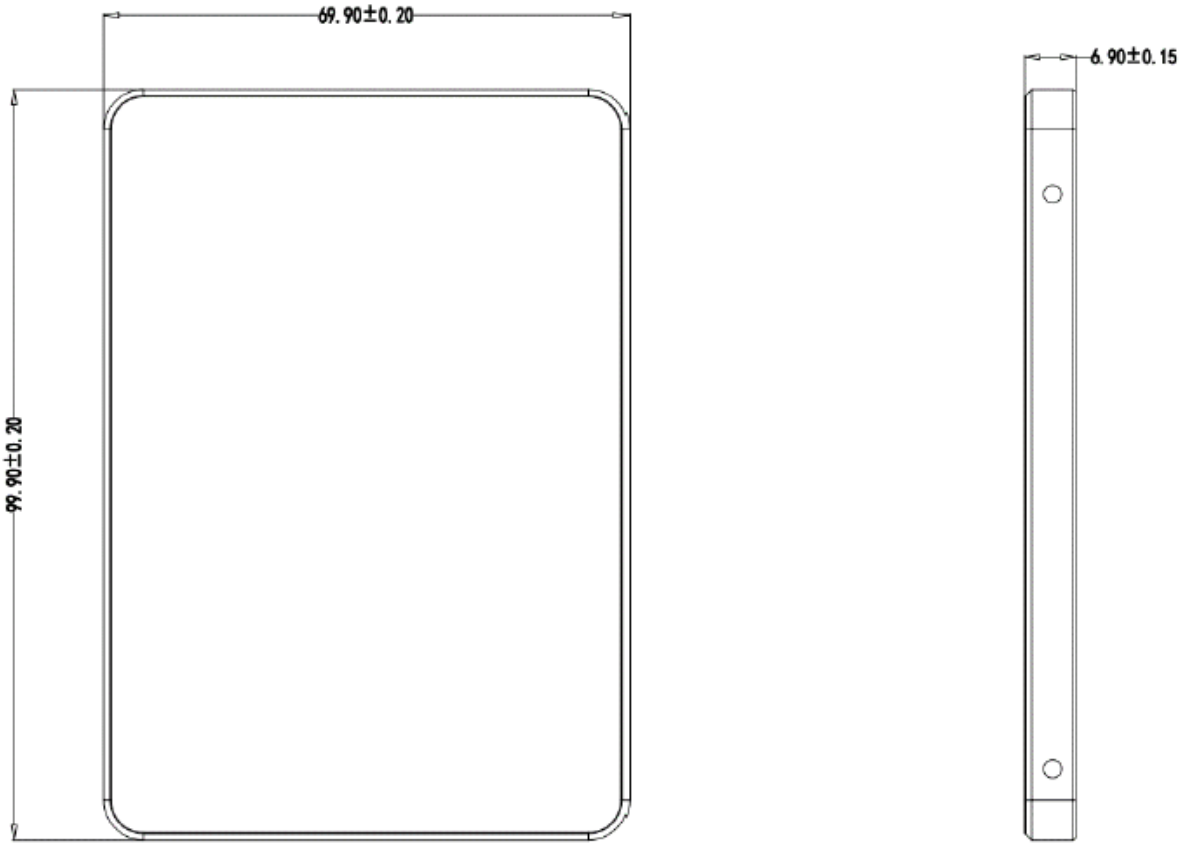

Figure 5-1 Physical Dimensions

6. Product Ordering Information

The following table lists the available models of SMI-Sxxx-AC series which are in mass production or will be in mass production. Consult your sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Capacity	Advantech PN	Description	MPN
128GB	SMI-S128-AC	Semi Industrial 2.5" SSD TLC 128G 0~70C	AP2HPBSS25A-2501
256GB	SMI-S256-AC	Semi Industrial 2.5" SSD TLC 256G 0~70C	AP2JPBSS25A-2501
512GB	SMI-S512-AC	Semi Industrial 2.5" SSD TLC 512G 0~70C	AP2KPBSS25A-2501
1TB	SMI-S1TB-AC	Semi Industrial 2.5" SSD TLC 1TB 0~70C	AP3APBSS25A-2501

Appendix: Label Specifications

The illustration below is for reference only. For the actual label content, please refer to the physical product.

Revision History

Revision	Description	Date
0.1	Preliminary release	6/19/2025
1.0	Updated NAND Flash Type from 3D TLC to 3D NAND on the Specifications Overview page	8/5/2025
1.1	- Updated NAND Flash Type from 3D NAND to 3D TLC on the Specifications Overview page on the Specifications Overview page - Updated endurance rating on the Specifications Overview page and Table 1-3	8/22/2025
1.2	- Updated mechanical dimensions and illustration at 5. Mechanical Specifications	6/1/2026